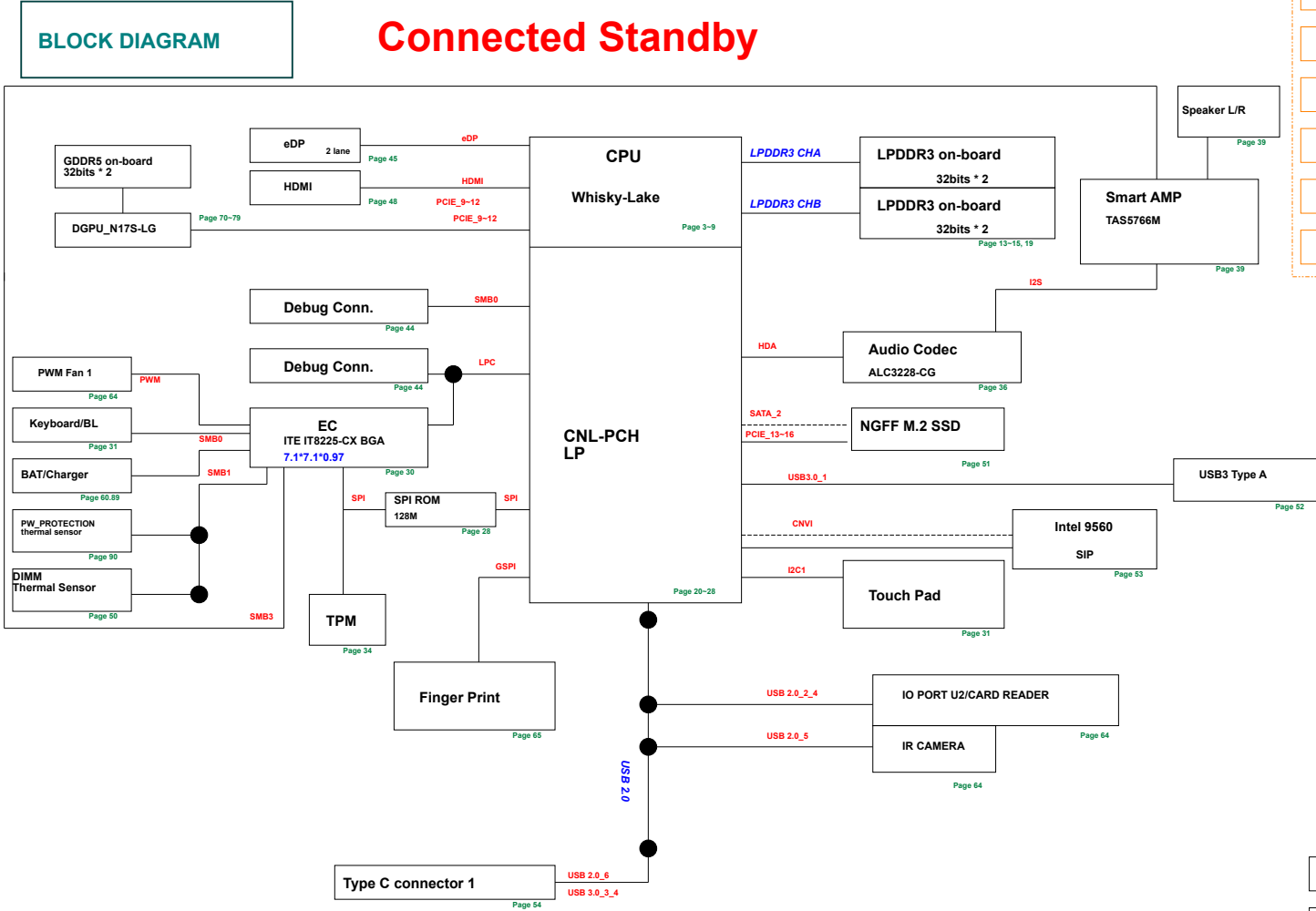


UX334F Series SCHEMATIC Revision 2.0

PAGE	Content
1	Block Diagram
2	System Setting
3	CPU_DISPLAY
4	CPU_DDR3L
5	CPU_LPC, SPI, SMB, CLINK
6	CPU_POEWR
7	CPU_XDP
8	CPU_MISC, JTAG, CLK
9	CPU_CFG, RSVD
10	CPU_POWER_CAP
11	TBT_Alpine-Ridge
12	TBT&TSP65982&Type_C_port1
13	LPDDR3_TERMINATION
14	LPDDR3_ON-BOARD_A
15	LPDDR3_ON-BOARD_B
16	
19	LPDDR3_CA_DQ VOLTAGE
20	CPU_PCH_CFG, DISPLAY
21	CPU_PCH_CGPIO, LPIO, MISC
22	CPU_PCH_SATA, JTAG, AUDIO, RTC
23	CPU_PCH_PCIE, USB
24	CPU_PCH_CLOCK SIGNALS
25	CPU_PCH_SYS_POWER
26	CPU_PCH_POEWR, GND
27	CPU_PCH_POEWR, GND
28	PCH_SPI ROM, OTH, TPM
29	D_DOOR_OPEN
30	KBC_IT8995
31	EC_KB_TP
32	Lid Switch
37	AUD_ALC295
39	AUD_SMA_TSA5766M
41	TBT_TSP65982&Type_C_Port2
44	BUG_Debug
45	CRT_LCD Panel_CMOS_DMIC
50	FAN
51	M2_SSD
52	
53	
56	LED_Indicator
57	DSG_Discharge
58	PRO_PROTECT
60	DC_DC & BAT Conn.
62	ME_Conn & Skew Hole
63	EMI_RF Reserve
64	B TO B CONN
65	
67	
68	
69	
70	
71	
72	
73	
74	
75	
76	
77	
80_PW_IMVP8 (1)	
81_PW_IMVP8 (2)	
83_PW_+1.2V/ +1.8VSUS	
84_PW_+1.0VSUS	
87_PW_+3VADSW/+5VSUS	
88_PW_LOAD SWITCH	
89_PW_CHARGER(ISL9237 (NVDC +HPB))	
90_PW_PROTECTION	



Power

- PW_IMVP8 (Page 80,81)
- +3VADSW/+5VSUS (Page 87)
- /+1.05VSUS+1.8VSUS (Page 83)
- +1.2V / +VTT / +1.8V (Page 86)
- Charger (Page 89)
- Load Switch (Page 88)

Discharge Circuit (Page 57)

Reset Circuit (Page 25)

DC & BATT. Conn. (Page 60)

Skew Holes (Page 62)

EMI RF reserve (Page 63)

PCB_I2XX_GPIO	Use As	Signal Name	Power on Default Status	IOLE ET Pull-up / down	Power
GFP_A0	Natival	NC_DNR		EXT PD 10K	+3VS
GFP_A1	Natival	LPC_ADD			
GFP_A2	Natival	LPC_AD1			
GFP_A3	Natival	LPC_ADD			
GFP_A4	Natival	LPC_ADD			
GFP_A5	Natival	LPC_FRAME#			
GFP_A6	Natival	INT_BERR0		EXT PD 10K	+3VS
GFP_A7	Natival	PIR0A#		EXT PD 10K	+3VS
GFP_A8	Natival	PM_CLKRUN#		EXT PD 8.2K	+3VS
GFP_A9	Natival	CLK_RMPC1_PCH			
GFP_A10	Natival	CLK_DM00			
GFP_A11	GPIO	N/A			
GFP_A12	GPIO	N/A			
GFP_A13	Natival	ME_SioPwrdnAck_B		EXT PD 10K	+3VS02
GFP_A14	Natival	R02_STAT#			
GFP_A15	Natival	SDR0ACH_#			
GFP_A16	GPIO	N/A			
GFP_A17	GPIO	N/A			
GFP_A18	GPIO				
GFP_A19	GPIO				
GFP_A20	GPIO				
GFP_A21	GPIO				
GFP_A22	GPIO				
GFP_A23	GPIO				
GFP_B0	GPIO				
GFP_B1	GPIO				
GFP_B2	GPIO	N/A			
GFP_B3	GPIO	N/A			
GFP_B4	GPIO	N/A			
GFP_B5	GPIO	N/A			
GFP_B6	Natival	CLK_REQ_S0D#		EXT PD 10K	+3VS
GFP_B7	GPIO	N/A			
GFP_B8	GPIO	N/A			
GFP_B9	GPIO	N/A			
GFP_B10	Natival	CLK_REQ_V0A#		EXT PD 10K	+3VS
GFP_B11	GPIO	MHW_PWDEN		EXT PD 20K	+3VS02
GFP_B12	Natival	PCH_SLP_S0#		EXT PD 810K	+3VS02
GFP_B13	Natival	P2T_RST#			
GFP_B14	GPIO	N/A			
GFP_B15	Natival	N/A		EXT PD 810K	+3VS
GFP_B16	Natival	N/A			
GFP_B17	Natival	N/A			
GFP_B18	Natival	N/A			
GFP_B19	GPIO	N/A			
GFP_B20	GPIO	GPU_EVNT0#		EXT PD 10K	+3VS
GFP_B21	GPIO	GC5_FB_EN_3.3			
GFP_B22	GPIO	N/A		EXT PD 100K	+3VS02
GFP_B23	Natival	BMGLALERT#		EXT PD 2.2K	+3VS02
GFP_C0	Natival	DMB_CR		EXT PD 2.2K	+3VS02
GFP_C1	Natival	DMB0_DATA		EXT PD 2.2K	+3VS02
GFP_C2	GPIO	N/A			
GFP_C3	Natival	BMGL0_CR (NC)		EXT PD 2.2K	+3VS02
GFP_C4	Natival	BMGL0_DATA (NC)		EXT PD 2.2K	+3VS02
GFP_C5	GPIO	GPIO_C5		EXT PD 8T 8m/PD 810K	+3VA_DSM
GFP_C6	Natival	BMGL0_CR (NC)		EXT PD 2.2K	+3VS02
GFP_C7	Natival	BMGL0_DATA (NC)		EXT PD 2.2K	+3VS02
GFP_C8	GPIO	N/A			
GFP_C9	GPIO	N/A			
GFP_C10	GPIO	N/A			
GFP_C11	GPIO	N/A			
GFP_C12	GPIO	D1NH_BEL0		EXT PD/PD 10K	+3VS02
GFP_C13	GPIO	D1NH_BEL1		EXT PD/PD 10K	+3VS02
GFP_C14	GPIO	D1NH_BEL2		EXT PD/PD 10K	+3VS02
GFP_C15	GPIO	FP_RST#		EXT PD 10K	+3VS
GFP_C16	GPIO	N/A			
GFP_C17	GPIO	N/A			
GFP_C18	Natival	12CL1_S0A_PCH_P0A0		EXT PD 4.7K	+3VS
GFP_C19	Natival	12CL1_SCL_PCH_P0A0		EXT PD 4.7K	+3VS
GFP_C20	GPIO	GDPU_PWD0#			
GFP_C21	GPIO	GDPU_RST#		EXT PD 10K	
GFP_C22	GPIO	GDPU_PWR_R0#		EXT PD 10K	+3VS02
GFP_C23	GPIO	N/A		EXT PD 10K	
GFP_C0	GPIO	N/A			
GFP_D1	GPIO	N/A			
GFP_D2	GPIO	N/A			
GFP_D3	GPIO	N/A			
GFP_D4	GPIO	N/A			
GFP_D5	GPIO	N/A			
GFP_D6	GPIO	N/A			
GFP_D7	GPIO	N/A			
GFP_D8	GPIO	N/A			
GFP_D9	GPIO	PCB_ID0		EXT PD10K/PD 10K	+3VS
GFP_D10	GPIO	FP_RST_#R#		EXT PD 1K	
GFP_D11	GPIO	N/A			
GFP_D12	GPIO	EF1D_M0B1		EXT PD 100K	+3VS02
GFP_D13	GPIO	TOUCHPAD_INT#		EXT PD 10K	+3VS
GFP_D14	GPIO	N/A			
GFP_D15	GPIO	N/A			
GFP_D16	GPIO	FP_RST_INT			
GFP_D17	GPIO	N/A			
GFP_D18	GPIO	N/A			
GFP_D19	Natival	DMIC_CLK_PCH_X1			
GFP_D20	Natival	DMIC_DATA_PCH			
GFP_D21	GPIO	N/A			
GFP_D22	GPIO	N/A			

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PCB_I2XX_GPIO	Use As	Signal Name	Power on Default Status	IOLE ET Pull-up / down	Power
GFP_D23	GPIO	N/A			
GFP_E0	GPIO	N/A			
GFP_E1	GPIO	N/A			
GFP_E2	Natival	MEATA_NPCLE_DEV#		EXT PD 10K	+3VS
GFP_E3	GPIO	N/A			
GFP_E4	GPIO	N/A			
GFP_E5	GPIO	N/A			
GFP_E6	NATIVAL	HATA2_DEVSLP			
GFP_E7	GPIO	N/A			
GFP_E8	GPIO	N/A			
GFP_E9	NATIVAL	USB_SC1_#		EXT PD 10K	+3VS02
GFP_E10	NATIVAL	USB_SC1_#		EXT PD 10K	+3VS02
GFP_E11	NATIVAL	USB_SC1_#		EXT PD 10K	+3VS02
GFP_E12	NATIVAL	USB_SC1_#		EXT PD 10K	+3VS02
GFP_E13	GPIO	N/A			
GFP_E14	NATIVAL	SDR0_P		EXT PD 1K	+3VS
GFP_E15	GPIO	EXT_DM0#		EXT PD 10K	+3VS
GFP_E16	GPIO	EXT_DM0#		EXT PD 10K	+3VS
GFP_E17	NATIVAL	SDP_XPD_DSM		EXT PD 100K	+3VS
GFP_E18	GPIO	N/A			
GFP_E19	GPIO	N/A			
GFP_E20	NATIVAL	SDR0_SCL_PCH		EXT PD 2.2K	+3VS
GFP_E21	NATIVAL	SDR0_GSA_PCH		EXT PD 2.2K	+3VS
GFP_E22	GPIO	N/A			
GFP_E23	GPIO	N/A			
GFP_F0	GPIO	N/A			
GFP_F1	GPIO	N/A			
GFP_F2	GPIO	N/A			
GFP_F3	GPIO	N/A			
GFP_F4	NATIVAL	CHP_R01_0T		EXT PD 10K	+1.8VS02
GFP_F5	NATIVAL	CHP_R01_0T		EXT PD 20K	+1.8VS02
GFP_F6	NATIVAL	CHP_R01_0T		EXT PD 20K	+1.8VS02
GFP_F7	NATIVAL	CHP_R01_0T		EXT PD 10K	+1.8VS02
GFP_F8	GPIO	N/A			
GFP_F9	GPIO	N/A			
GFP_F10	GPIO	N/A			
GFP_F11	GPIO	N/A			
GFP_F12	GPIO	N/A			
GFP_F13	GPIO	N/A			
GFP_F14	GPIO	N/A			
GFP_F15	GPIO	N/A			
GFP_F16	GPIO	N/A			
GFP_F17	GPIO	N/A			
GFP_F18	GPIO	N/A			
GFP_F19	GPIO	N/A			
GFP_F20	GPIO	N/A			
GFP_F21	GPIO	N/A			
GFP_F22	GPIO	N/A			
GFP_F23	GPIO	N/A			
GFP_G0	GPIO	N/A			
GFP_G1	GPIO	N/A			
GFP_G2	GPIO	N/A			
GFP_G3	GPIO	N/A			
GFP_G4	GPIO	N/A			
GFP_G5	GPIO	N/A			
GFP_G6	GPIO	N/A			
GFP_G7	GPIO	N/A			
GFP0	Natival	PL_R0T0N0_#		EXT PD 8.2K	+3VA_DSM
GFP1	Natival	HE_AC_PWDEN0_PCH		EXT PD 100K	+3VA_DSM
GFP2	GPIO	PCB_DP024 (NC)		EXT PD 10K	+3VA_DSM
GFP3	Natival	PL_PWDEN0_PCH			
GFP4	Natival	PL_S0R0#		EXT PD 100K	
GFP5	Natival	PL_R0CK#		EXT PD 100K	
GFP6	GPIO	SLP_AB (NC)			
GFP7	Natival	DP0T		EXT PD 100K	+3VA_DSM
GFP8	Natival	PH0_CR			
GFP9	GPIO	N/A			
GFP10	Natival	S1P_254 (NC)			
GFP11	Natival	L0A0_PWDEN (NC)		EXT PD 10K	+3VA_DSM
GFP_R0	GPIO	N/A			
GFP_R1	Natival	RF_R0R0T_0		EXT PD 10K	
GFP_R2	Natival	CLKRQ0		EXT PD 10.7K	
GFP_R3	GPIO	N/A			
GFP_R4	GPIO	N/A			
GFP_R5	GPIO	N/A			
GFP_R6	GPIO	N/A			
GFP_R7	GPIO	N/A			
GFP_R8	GPIO	N/A			
GFP_R9	GPIO	N/A			
GFP_R10	GPIO	N/A			
GFP_R11	GPIO	N/A			
GFP_R12	GPIO	N/A			
GFP_R13	GPIO	N/A			
GFP_R14	GPIO	N/A			
GFP_R15	GPIO	N/A			
GFP_R16	GPIO	N/A			
GFP_R17	GPIO	N/A			
GFP_R18	Natival	GPU_C15_GATE#		EXT PD 10K	+3VA_DSM
GFP_R19	GPIO	N/A			
GFP_R20	GPIO	N/A			
GFP_R21	Natival	GPFC_R21		EXT PD 4.7K	+3VA_DSM
GFP_R22	GPIO	N/A			
GFP_R23	GPIO	GPFC_R23			

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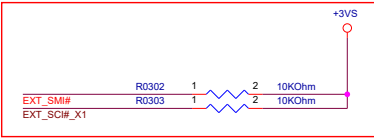
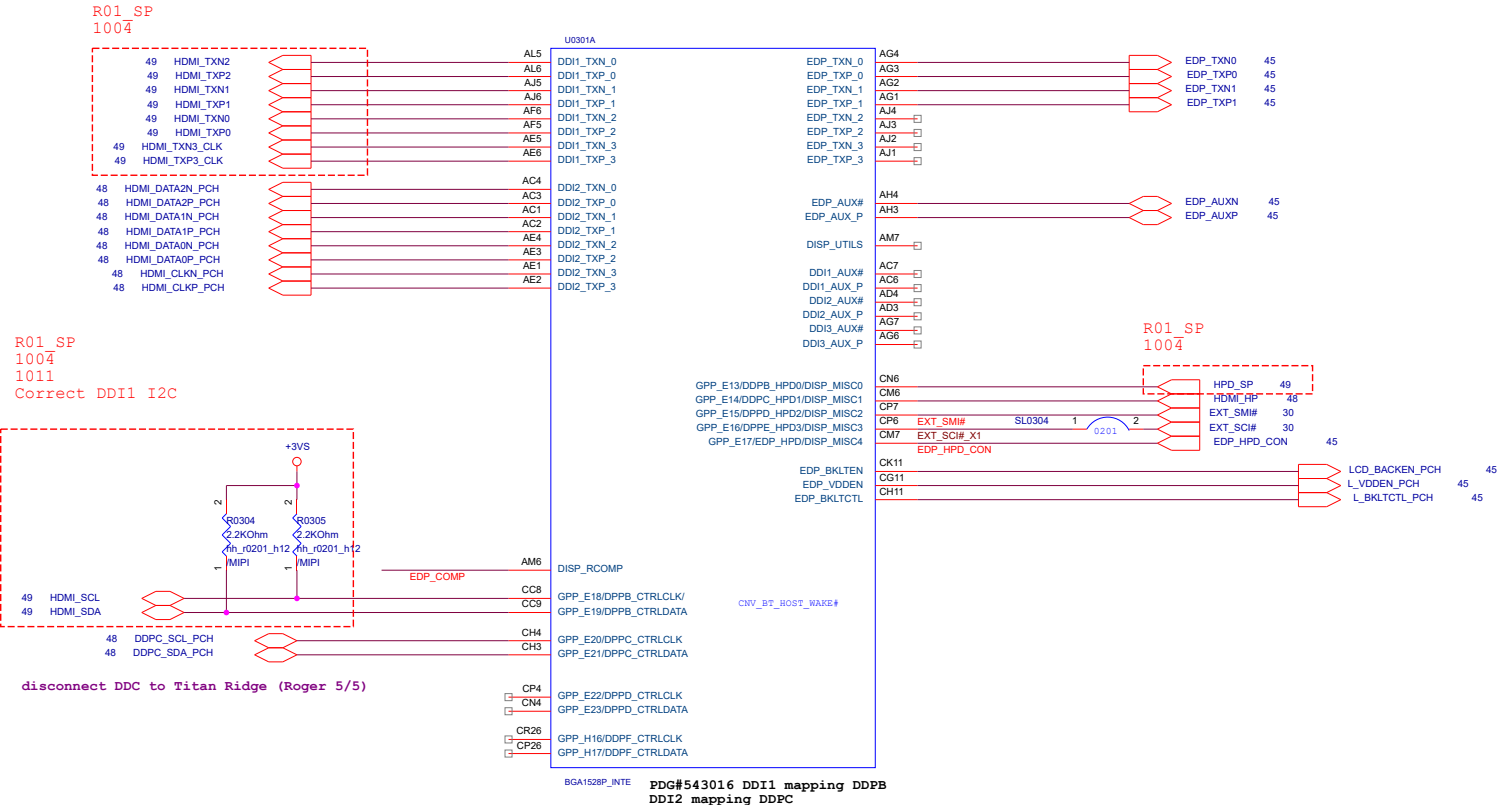
*1: NC config GPIO Function output

Pin Name	Config	Signal Name	Default status	Ext Pull up / down
GPAD0	0	PW1_LED		
GPAD1	0D	DM0_LED0	HIGH	
GPAD2	0D	DM0_LED1_LED0	HIGH	
GPAD3	0	N/A	LOW	
GPAD4	0	N/A	LOW	
GPAD5	ALIC	PW1_LED0	LOW	
GPAD6	ALIC	PW1_LED0_PWD0	LOW	
GPAD7	0	N/A	HIGH	
GPAD8	ALIC	NC_R0T0N	HIGH	EXT 100K
GPB1	1	LED_DM0	LOW	EXT 100K PD
GPB2	0D	N/A	LOW	
GPB3	ALIC	PW1_LED	HIGH	EXT 100K PD
GPB4	1	PL_R0T0N	HIGH	
GPB5	0	N/A	LOW	
GPB6	0D	NC_R0T0N	LOW	EXT 10K PD
GPB7	0	LED_010000010_0	LOW	
GPB1	ALIC	DM0_LED	LOW	EXT 4.7K PD
GPB3	ALIC	DM0_LED	LOW	EXT 4.7K PD
GPB4	1	PL_PWDEN0#	HIGH	
GPB5	1	PL_S0R0#	LOW	EXT 100K PD
GPB6	1	PL_PWDEN0	LOW	EXT 100K PD
GPB7	ALIC	DM0_LED_DM0	HIGH	EXT 10K PD
GPB7	0	NC	LOW	
GPB7	1	PW1_LED_DM0	LOW	
GPB1	0	HE_AC_PWDEN0#	LOW	EXT 100K PD
GPB2	ALIC	R0T_RST_R0T0N	HIGH	
GPB3	0D	EXT_DM0	LOW	EXT 10K PD
GPB4	0D	EXT_DM0#	LOW	EXT 10K PD
GPB5	0	UP_DM0	LOW	EXT 100K PD
GPB6	ALIC	PW1_LED0	LOW	
GPB7	0	N/A	LOW	
GPB8	0	DM0_LED	HIGH	EXT 10K PD
GPB9	0	DM0_LED	HIGH	EXT 10K PD
GPB1	0	1.2V_DM0	LOW	
GPB2	0	3VS02_R0	LOW	EXT 10K PD 1K PD
GPB4	0	3VS02_R0	LOW	EXT 100K PD 1K PD
GPB5	0	3VS02_R0	LOW	EXT 100K PD
GPB6	0	3VS02_DM0	LOW	
GPB7	0	DM0_LED0	HIGH	EXT 10K PD
GPB8	0	DM0_LED0	HIGH	EXT 100K PD
GPB1	0	N/A		
GPB2	ALIC	P_PWDEN0_01K	LOW	EXT 4.7K PD
GPB3	ALIC	P_PWDEN0_01K	LOW	EXT 4.7K PD
GPB4	0	PL_PWDEN0	HIGH	
GPB5	0	PL_S0R0#	LOW	
GPB6	0	N/A	LOW	
GPB7	0	N/A	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
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GPB9	0	DM0_LED0	LOW	
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GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
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GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	
GPB1	0	DM0_LED0	LOW	
GPB2	0	DM0_LED0	LOW	
GPB3	0	DM0_LED0	LOW	
GPB4	0	DM0_LED0	LOW	
GPB5	0	DM0_LED0	LOW	
GPB6	0	DM0_LED0	LOW	
GPB7	0	DM0_LED0	LOW	
GPB8	0	DM0_LED0	LOW	
GPB9	0	DM0_LED0	LOW	

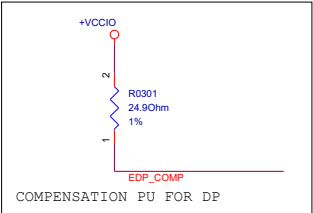
Display Port

A	EDP
B	
C	HDMI DP

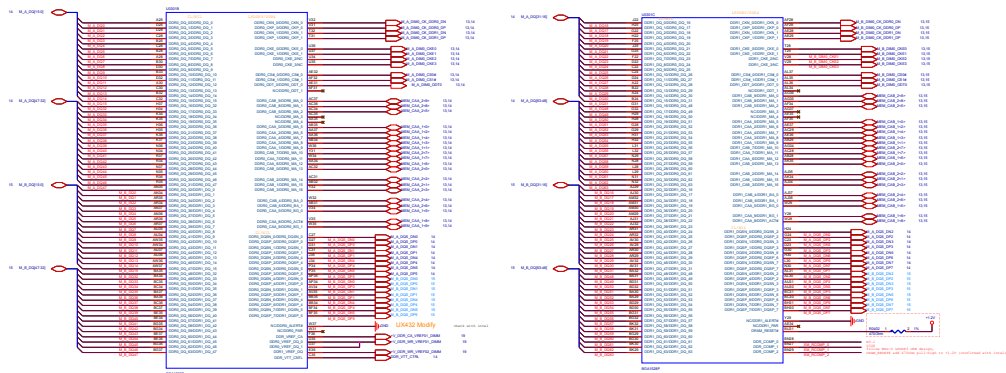
Intel Version	ASUS P/N
ES-0	01001-01540000



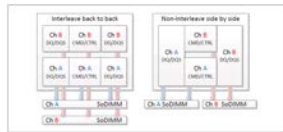
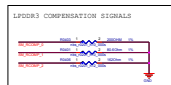
	HDMI
DDI_0	Lane2
DDI_1	Lane1
DDI_2	Lane0
DDI_3	CLK



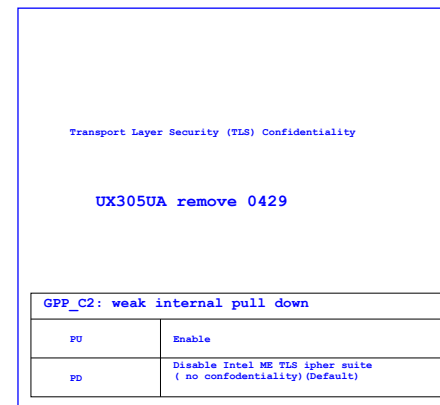
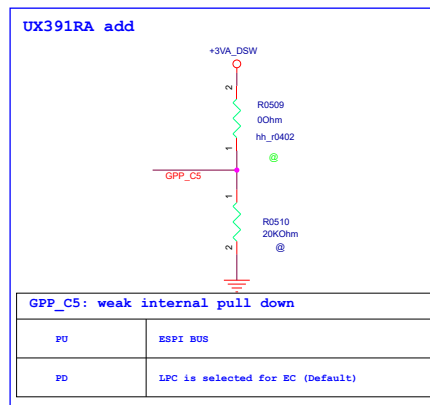
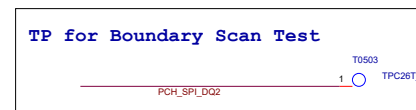
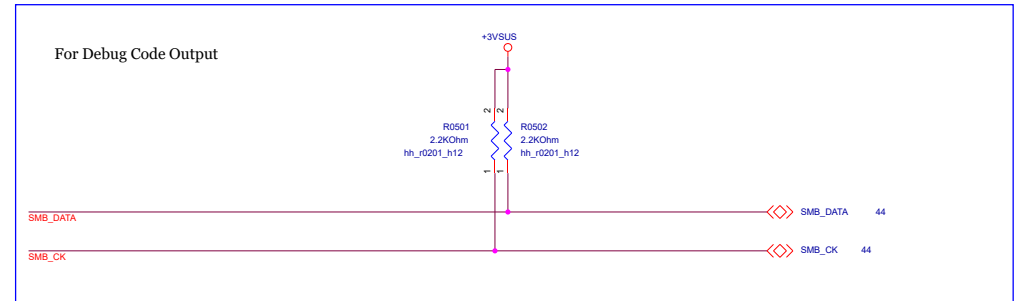
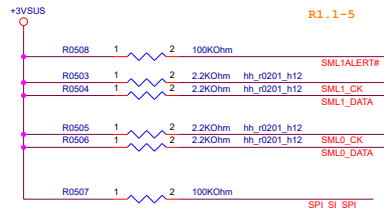
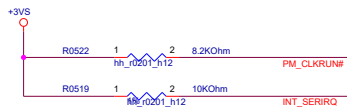
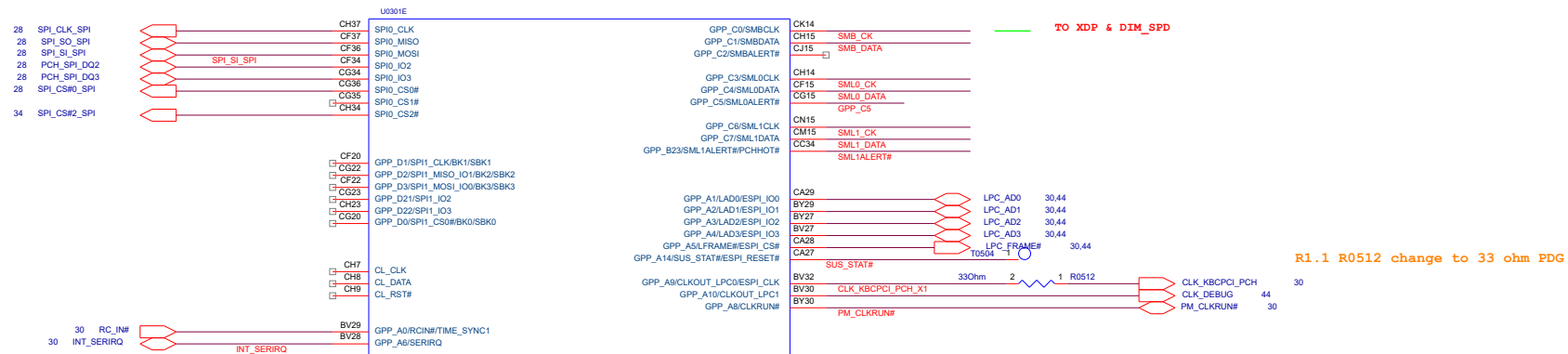
LPDDR3 Non-Interleaved



IL		NIL	
Channel	Byte	Channel	Byte
CD00	Byte0	CD00	Byte0
CD00	Byte1	CD00	Byte1
CD00	Byte2	CD00	Byte2
CD00	Byte3	CD00	Byte3
CD00	Byte4	CD01	Byte0
CD00	Byte5	CD01	Byte1
CD00	Byte6	CD01	Byte2
CD00	Byte7	CD01	Byte3
CD01	Byte0	CD00	Byte2
CD01	Byte1	CD00	Byte3
CD01	Byte2	CD00	Byte6
CD01	Byte3	CD00	Byte7
CD01	Byte4	CD01	Byte2
CD01	Byte5	CD01	Byte3
CD01	Byte6	CD01	Byte6

[illegible]

Platform	Config #	Tech	Topology	Max Freq	Memory Device	Device Baufuß	PCB Stack-up	2D/3D VLT
CFL-U LPDDR3	Chapter 4.2.1	LPDDR3	1R x32	1866/ 2133 ¹	SDP (1 x 32 desc)		HQ1 10L	
			2R x32	1866/ 2133 ¹	QOP (2 x 32 desc)	178	(1.7-3.1)	NIL
			2R x32	1866/ 2133 ¹	QOP(4 x 16 desc)			
	Chapter 4.2.2	LPDDR3	1R x64	1866/ 2133 ¹	QOP (2 x 32 desc)		HQ1 10L	
			2R x64	1866/ 2133 ¹	QOP (4 x 32 desc)	251	(3.3-3.4)	NIL



<Variant Name>



Project Name

UX334F

Rev

R2.0

Title : CPU_XDP

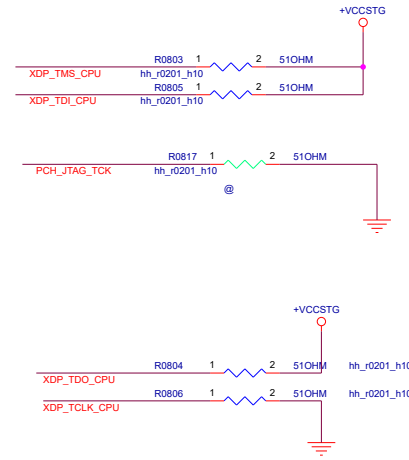
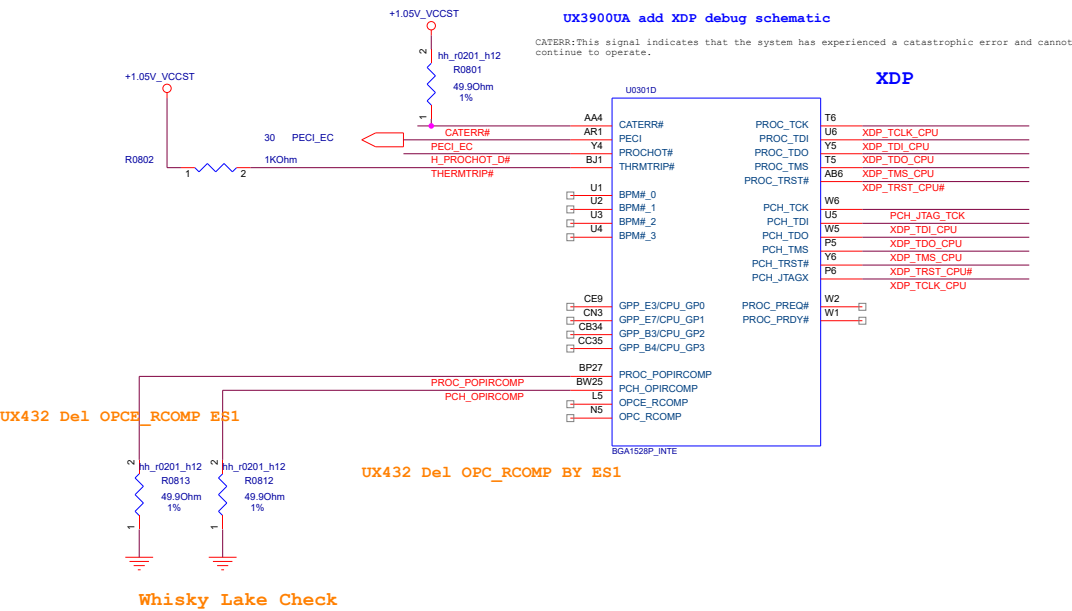
Size

C

Dept.: ASUSTeK COMPUTER INC. **Engineer:** Tony1_chang

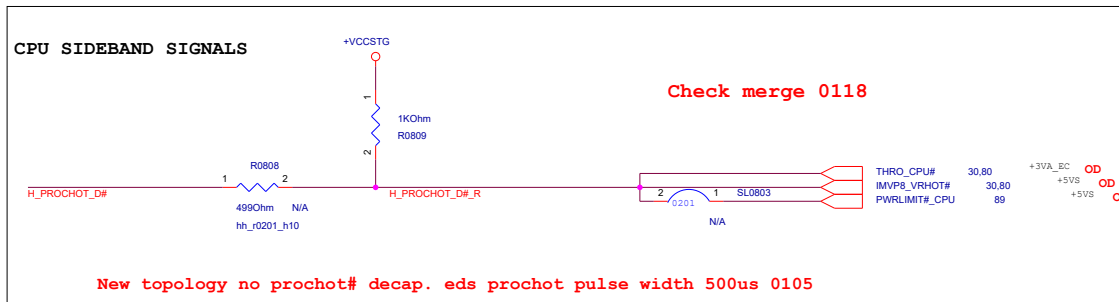
Date: Wednesday, April 10, 2019

Sheet 7 **of** 100

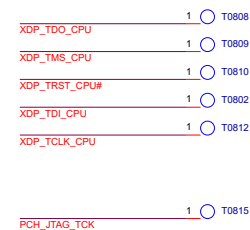


On Package Cache resistance Compensation
from processor: Refer to the appropriate platform
design guide for implementation details and values.
Unconnected for Processors without OPC.

No OPC Check remove 且R0811 R0810量測兩端為0V 0126



TP for Boundary Scan Test

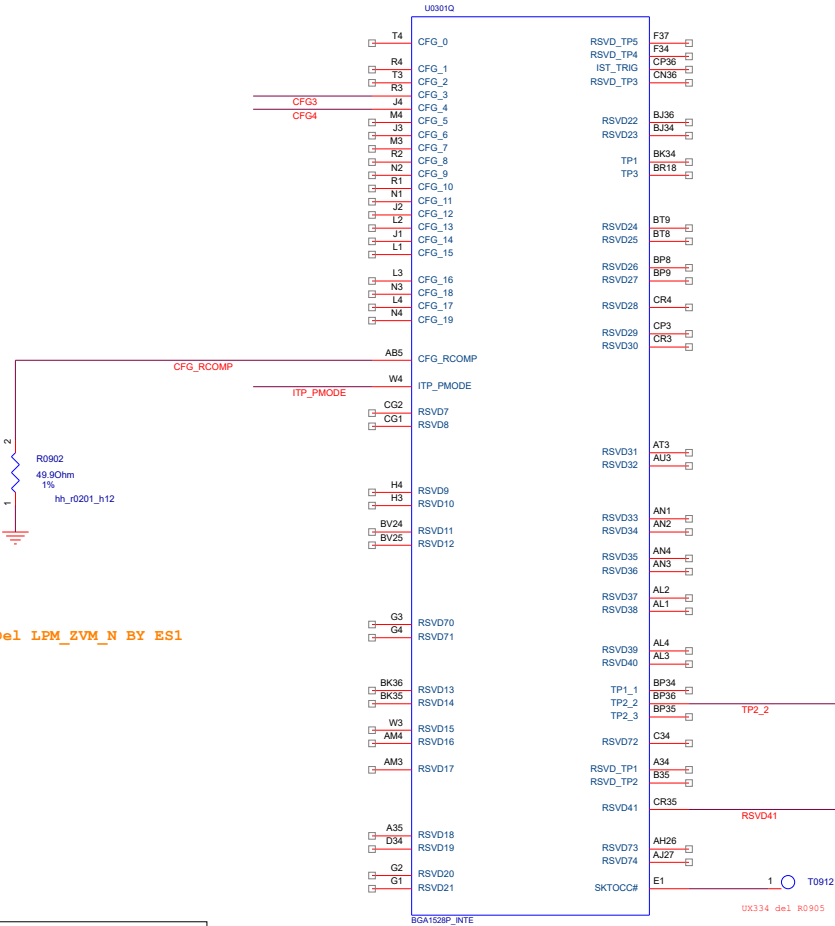


<Variant Name>

6.2 Reset and Miscellaneous Signals

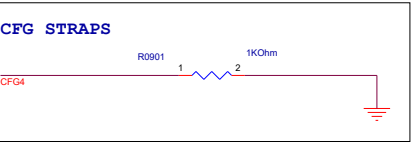
Table 6-5. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. <ul style="list-style-type: none">• CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:<ul style="list-style-type: none">— 1 = (Default) Normal Operation; No stall.— 0 = Stall.• CFG[1]: Reserved configuration lane.• CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.<ul style="list-style-type: none">— 1 = Normal operation— 0 = Lane numbers reversed.• CFG[3]: Reserved configuration lane.• CFG[4]: eDP enable:<ul style="list-style-type: none">— 1 = Disabled.— 0 = Enabled.• CFG[6:5]: PCI Express* Bifurcation<ul style="list-style-type: none">— 00 = 1 x8, 2 x4 PCI Express*— 01 = reserved— 10 = 2 x8 PCI Express*— 11 = 1 x16 PCI Express*• CFG[7]: PEG Training:<ul style="list-style-type: none">— 1 = (default) PEG Train immediately following RESET# de assertion.— 0 = PEG Wait for BIOS for training.• CFG[19:8]: Reserved configuration lanes.	I	GTL	SE	U - Processor Lines. CFG[2], CFG[6:5] and CFG[7] are not relevant for U - Processor Lines.
CFG_RCOMP	Configuration Resistance Compensation	N/A	N/A	SE	U-Processor Line
PROC_POPIRCOMP	POPPIO Resistance Compensation	N/A	N/A	SE	U-Processor Line
IST_TRIG	Impedance Spectrum Tool Trigger: trigger point to support debug of possible power issues. Refer to the appropriate processor Platform Design Guide (see Related Documents section) for complete implementation details.	O	GTL	SE	U-Processor Line



TP for Boundary Scan Test

TPC26T_50 1 T0910
CFG3
T0911 1
ITP_PMODE



	1	0	NOTE
CFG4	DISABLE	ENABLE	eDP ENABLE

+VCCCORE CPU - VCC DECAPS- Underneath the package

10 uF 0402 H=0.33 * 9
CAP above 10uF move to PWR page

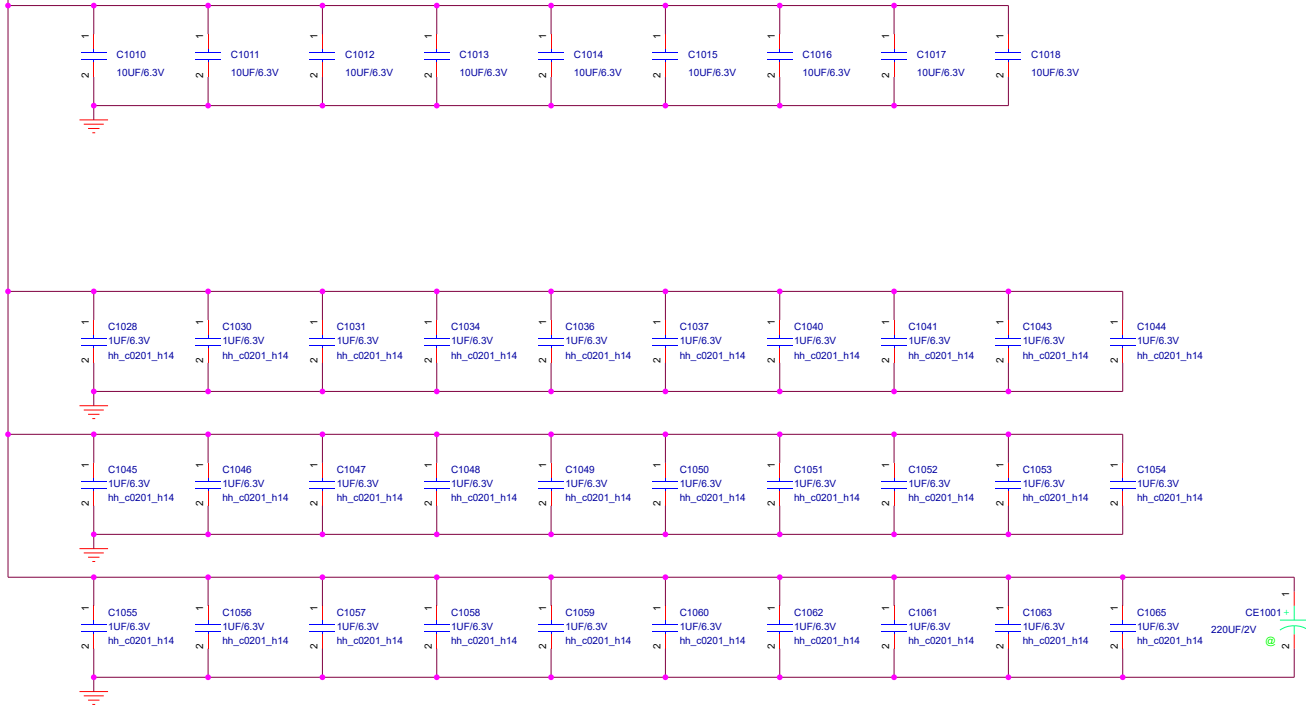


Table 11-2. Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCC _{CORE}		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
VCC _{GT}	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.
	15x 22uF 0603		Place as close to the package as possible
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	

+VCCCORE DeCap
0201 1uF/6.3V X5R h14 *30
0402 10uF/6.3V X5R h13 * 9



Project Name

UX334F

Rev

A3.0

Title : Intel Titan-Ridge

Drawn

Checked

Dept.:

ASUS COMPUTER INC.

Engineer:

Tony1_chang

Date: Wednesday, April 10, 2012

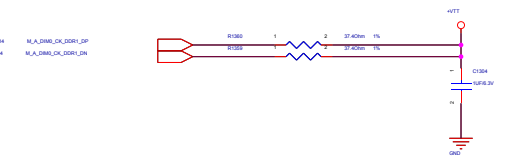
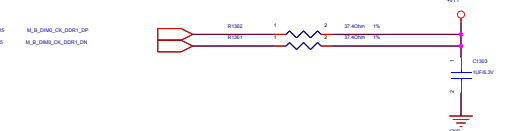
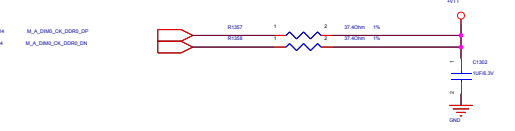
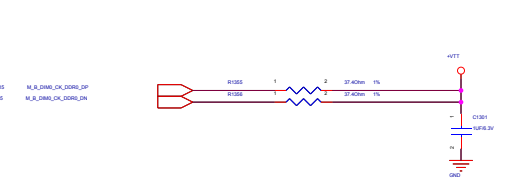
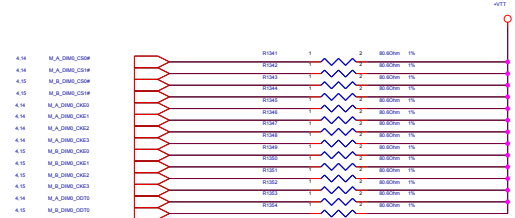
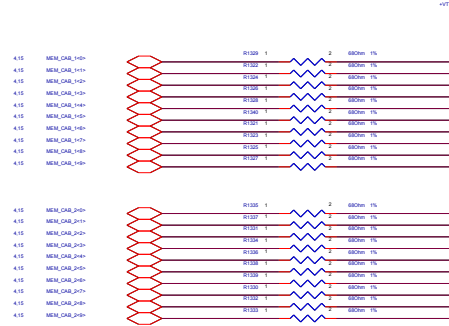
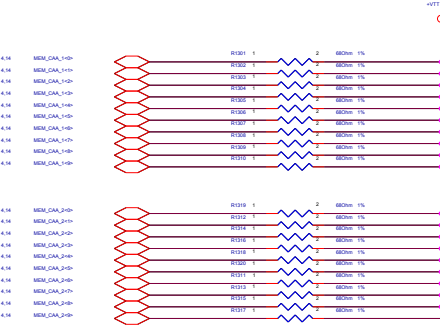
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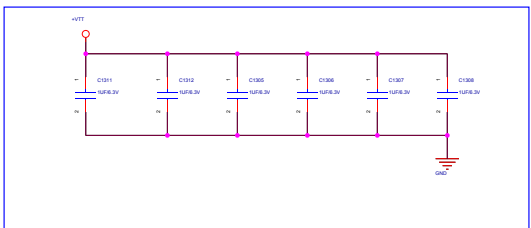
of

101



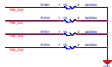


Close to LPDDR3 t erminatio n resistance (0402 siz e)



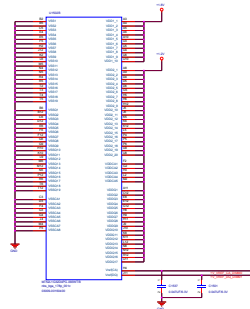
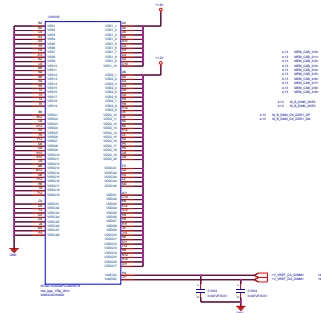
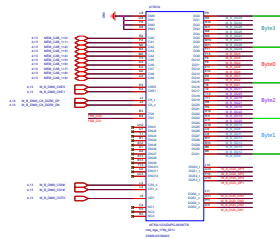
<Variant Name>

		Project Name	Rev
Title : LPDDR3_TERMINATION		R2.0	
Size Custom	Dept.: ASUStek COMPUTER INC. Engineer: Tony1_chang		
Date: Wednesday, April 10, 2019	Sheet	13	of 100



EPIDA & Samsung suggest 240 1% ohm

Intel suggest 243 1% ohm



<Variant Name>

ASUS		Project Name	Rev
UX334F			R2.0
Title : UPDORA_ON-BOARD_B			
0000	Dept.: ASUSTek COMPUTER INC.	Engineer: Tony1_chang	
D	Date: Wednesday, April 10, 2019		Sheet 15 of 100



Project Name

UX334F

Rev

R2.0

Title : **DDR3L SO-DIMM_B**

Size


C


Dept.: **NB1RD2EE2**

Engineer: **Tony1_chang**

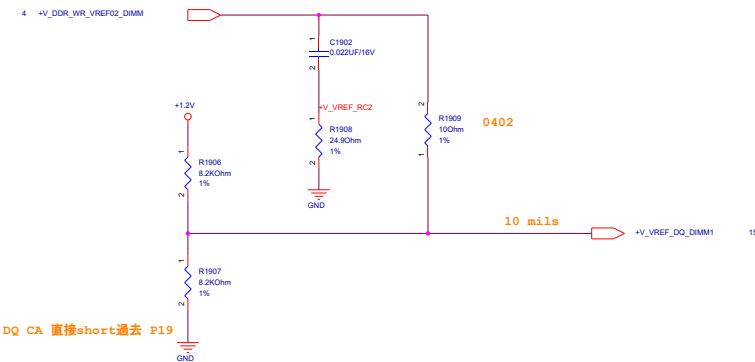
Date: **Wednesday, April 10, 2019**

Sheet 16 of 102

		Project Name		Rev
		UX334F		R2.0
Title : DDR3_ON-BOARD_B_L32				
Size	Dept.: NB1RD2EE2		Engineer:	Tony1_chang
C				
Date: Wednesday, April 10, 2019			Sheet	17 of 102

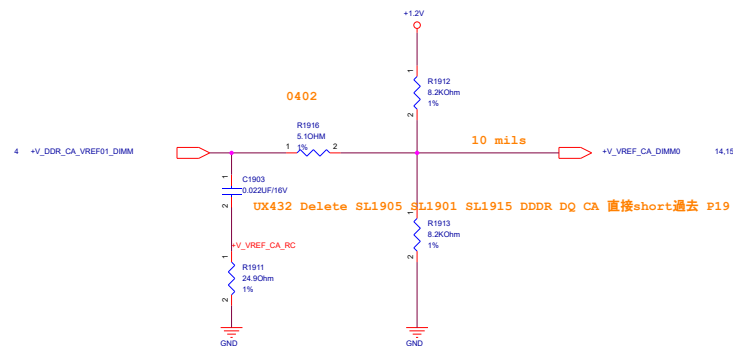
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		UX334F		R2.0
Title : DDR3_ON-BOARD_B_H32				
Size	Dept.: NB1RD2EE2			
C	Engineer:		Tony1_chang	
Date: Wednesday, April 10, 2019			Sheet	18 of 102

CHB - VREF DQ (All close to memory)

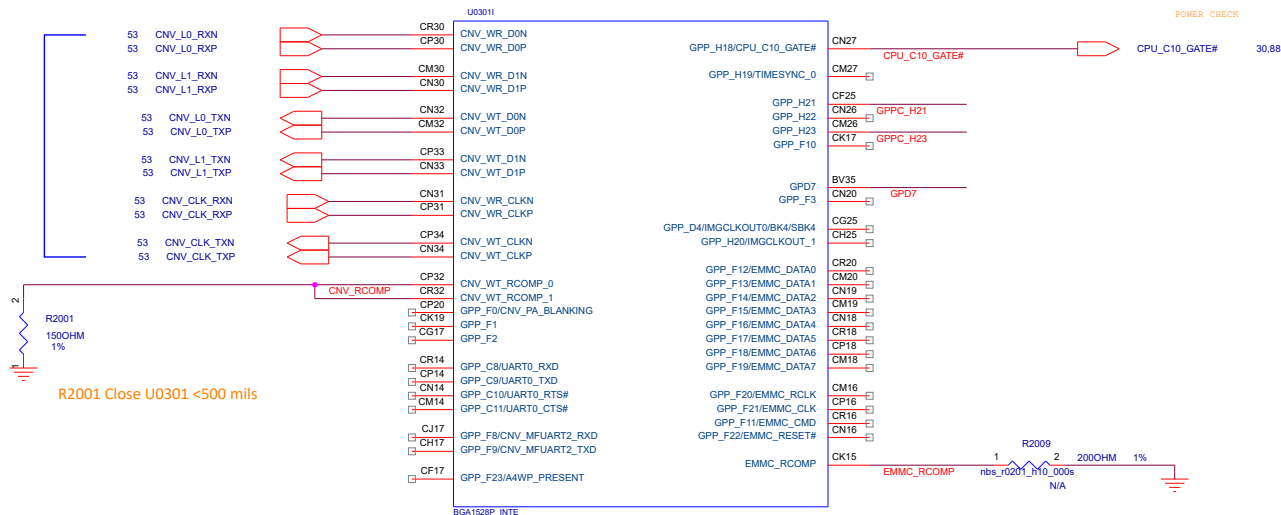


UX432 Delete SL1905 SL1901 SL1915 DDR DQ CA 直接short過去 P19

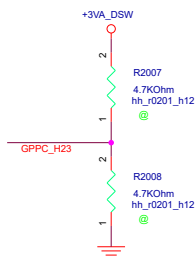
VREF_CA (All close to memory)



CNVi Wlan module



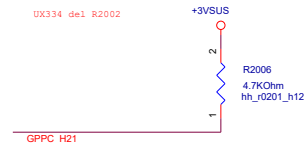
ESPI



GPPC_H23: INTERNAL WEAK PD

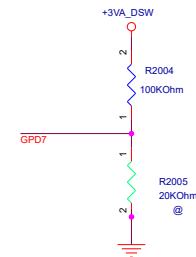
PU	SAF
PD	MAF

CFL CRB v0.8 page#44



GPPC_H21:

PU	24Mhz
PD	38.4/19.2MHZ



GPD7:

PD	XTAL INPUT IS SINGLE ENDED
PU	XTAL IS ATTACHED

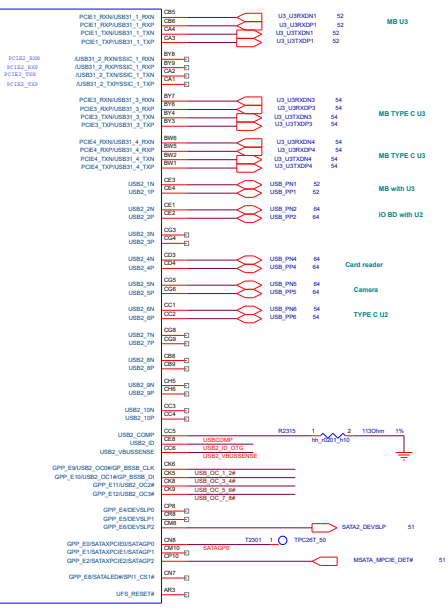
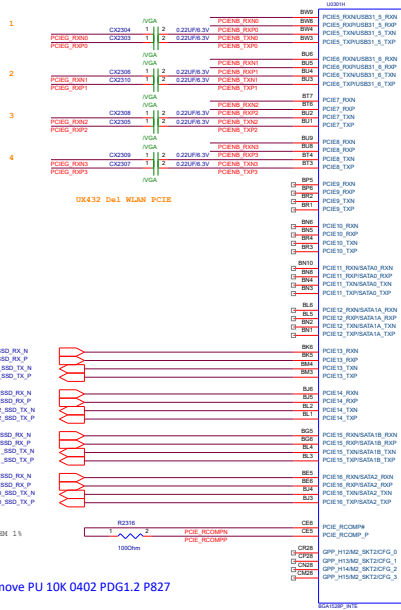
<Variant Name>



PCIE X4 same controller 0323

PCI-E* X1	PCIE USAGE DEFAULT/OPTION	Co-lay	Clock
PCIE 1	N/A		
PCIE 4	WLAN		
PCIE 6			
PCIE 8			
PCIE 10			Port0
PCIE 11			
PCIE 12	WLAN		Port3
PCIE 13	SSD	SATA SSD	
PCIE 14	SSD	SATA SSD	Port1
PCIE 15 / SATA 0	SSD	SATA SSD	
PCIE 16 / SATA 1	SSD	SATA SSD	

GPPA7 set to GPO remove PU 10K 0402 PDG1.2 P827

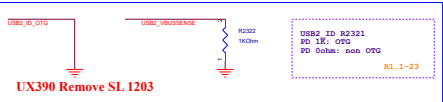


When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

R1.2 SATA_DEVSLP change to DEVSLEP2

SATA PORT2 0323

PDG1.2 P848 Unused SATAPG[2:0] pins can be left as no connect and need to be default to GPO functionality, refer to an unused GPO for termination guidance.



UX390 Remove SL 1203

Merge 0119

If unused, OC [4] pins require a pull-up to V3.3A with 8.2-10 KΩ resistors.



PE_DET SATA General Purpose



Variant Name

Project Name

ASUS UX334P

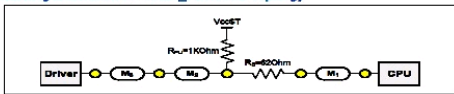
Title : CPU PCI PCIE USB SATA

Dept.: ASUS/SA COMPUTER INC. Engineer: Tony1_chang

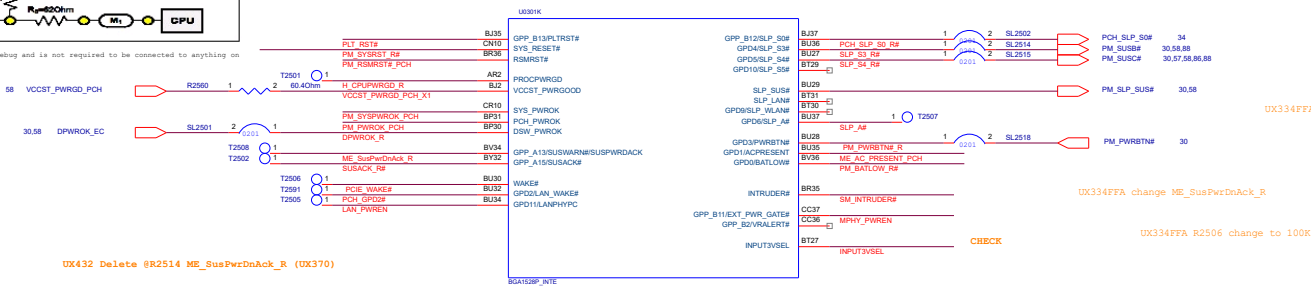
Date: Wednesday, April 10, 2019

Drawn: 23 of 100

Figure 7-18. Routing Illustration for VCCST_PWRGOOD Topology



PDG 1.2 P.572 PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the platform.

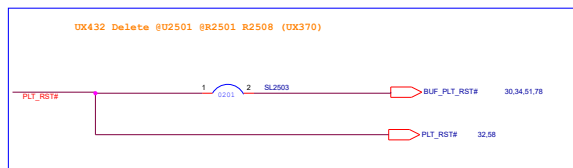


UX432 Delete @R2514 ME_SusPwrDnAck_R (UX370)

UX432 Delete PCIE WAKE#

UX432 Delete WLAN ON# Function GPD7

UX432 Delete @R2514 ME SusPwrDnAck R (UX370)



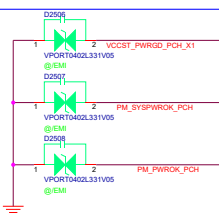
TP for Boundary Scan Test



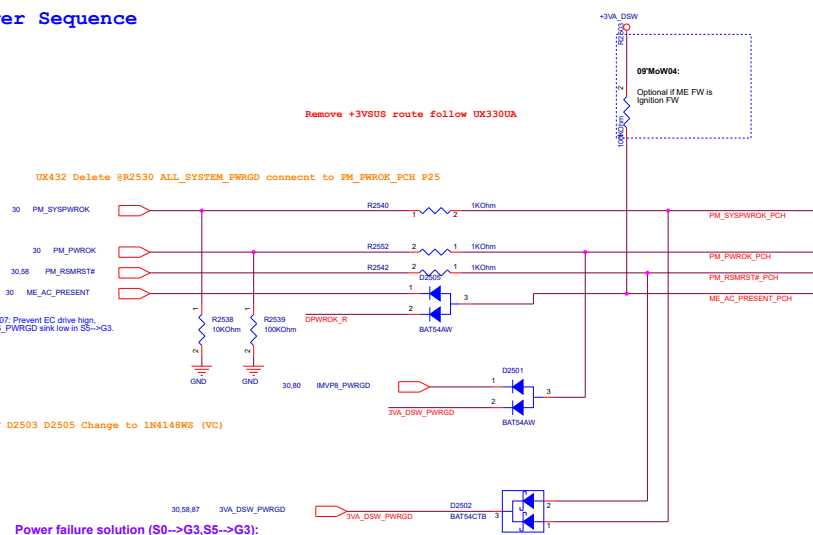
UX432 U2503 Change to D2504 Del @R2504 R2502 Add R2511 R2507

MS Gate for VCCIO

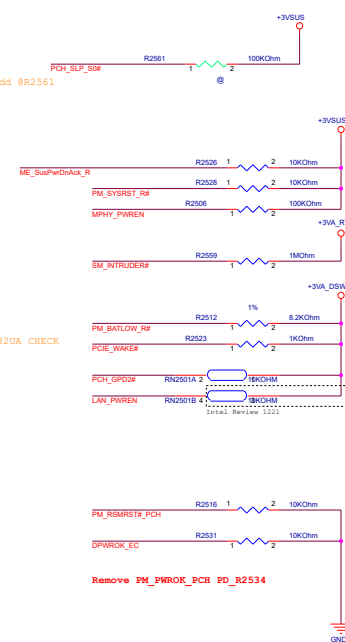
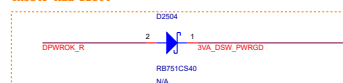
UX431 DEL D2504



Power Sequence



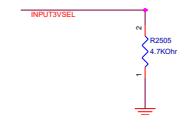
UX334F Add D2504



PCH STRAPS

Roger 3/21


UX334 del R2504

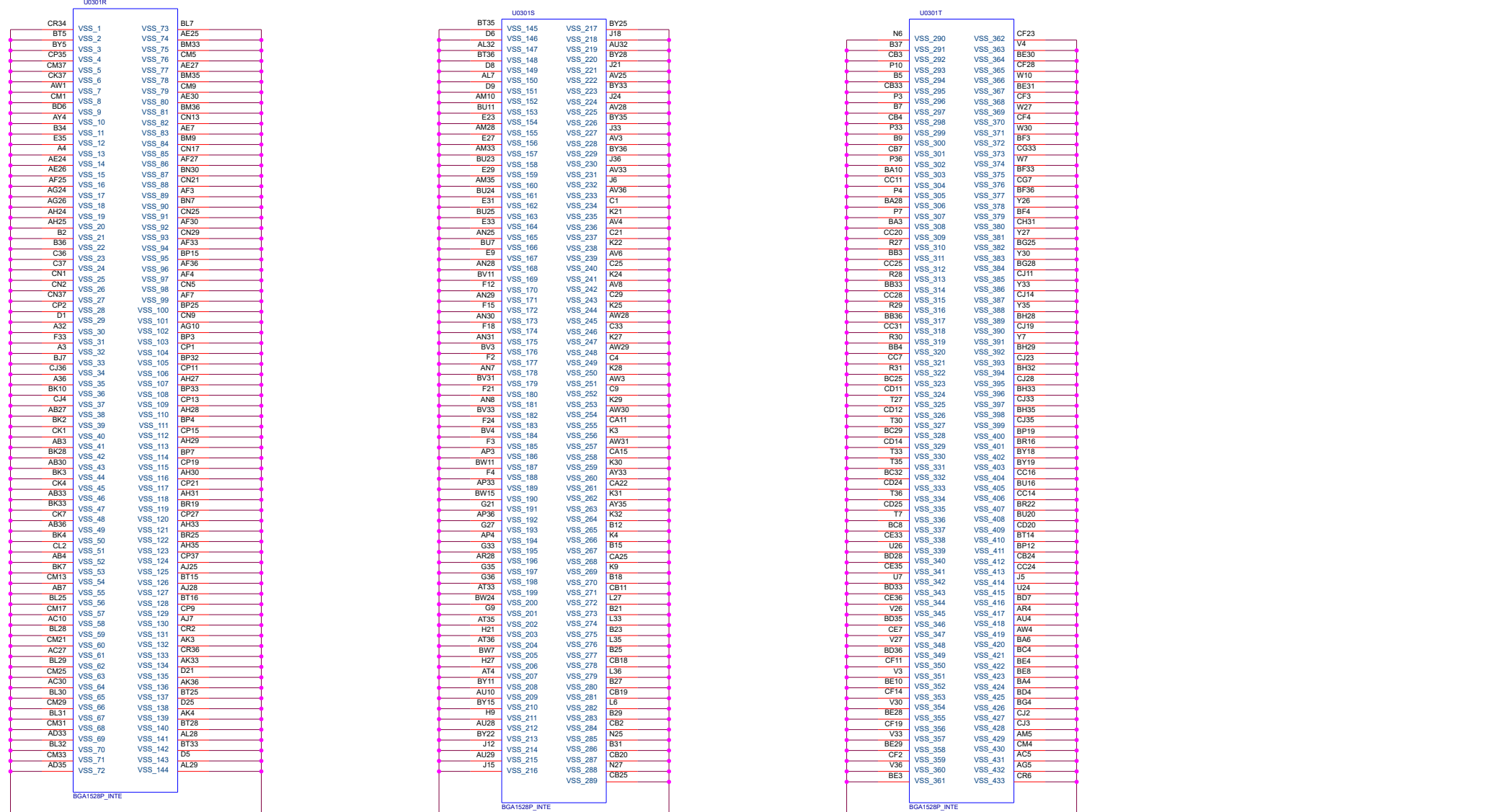


CFL: 3V SELECT STRAP

LOW	3.3V +/-5%
HIGH	3.0V +/-5%

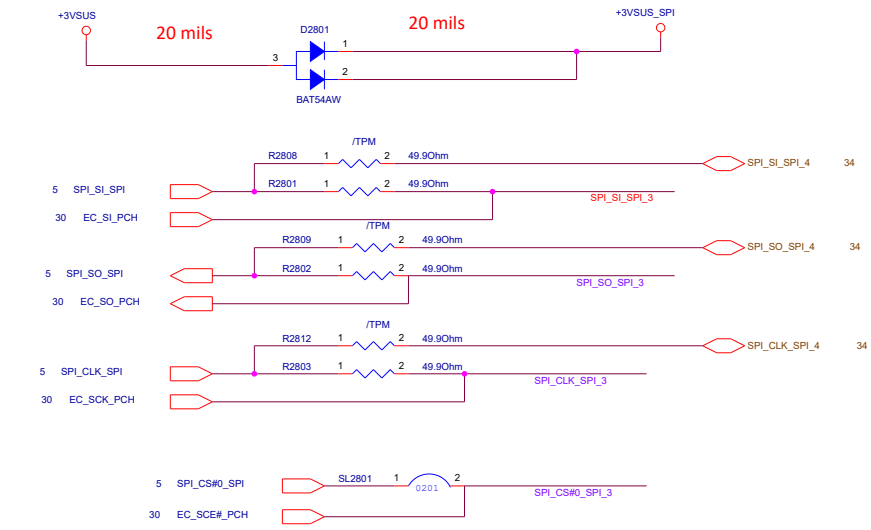
<Variant Name>

		Project Name UX334F		Rev R2.0	
Title : CPU_PCH_SYS_POWER					
Size Custom		Dept.: ASUS		Engineer: Tony1_chang	
Date: Wednesday, April 10, 2019		Sheet		25 of 102	

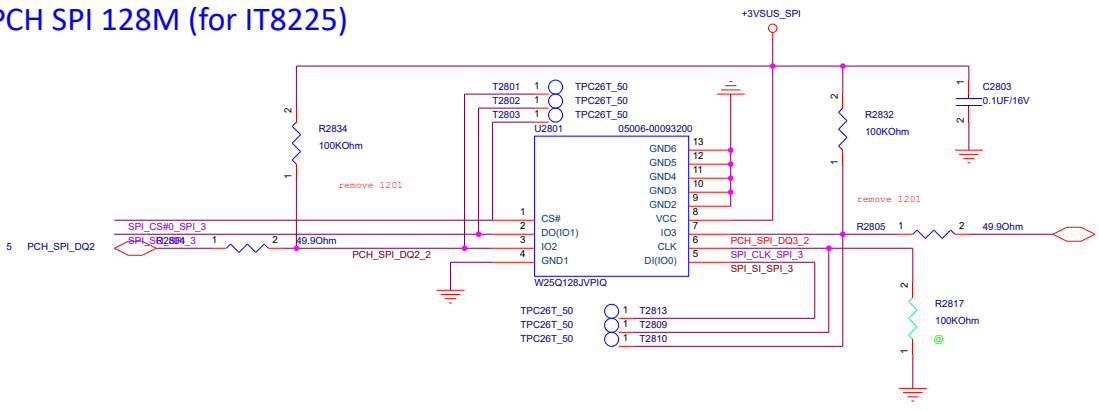


<Variant Name>

SPI PCH Power



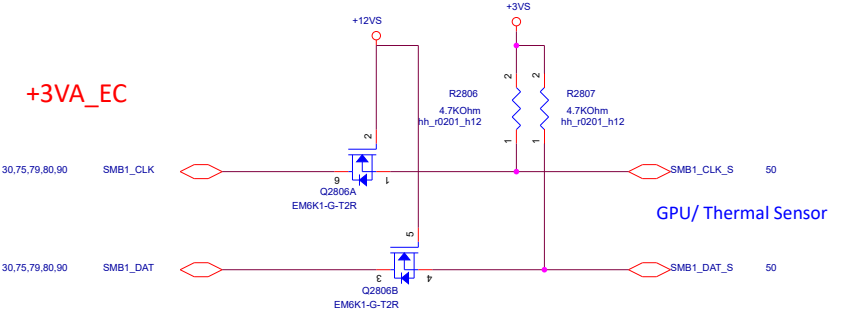
PCH SPI 128M (for IT8225)



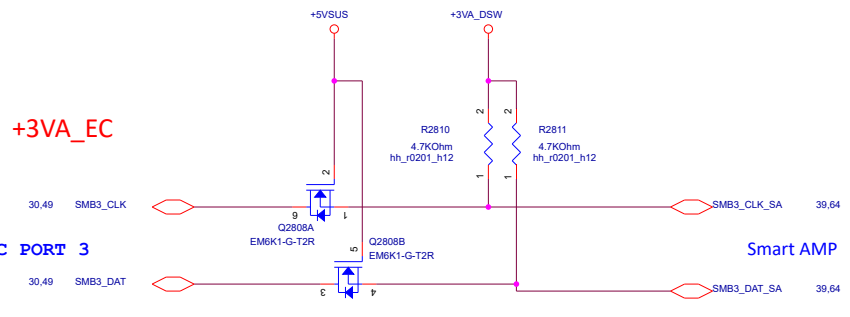
main : 05006-00093200
2nd: 05006-00093700

System Management Interface


EC PORT 1



EC PORT 3



UX334 move to screen pad

		Project Name		Rev
		UX334F		R2.0
Title : D_Door_Open				
Size	Dept.: ASUS		Engineer:	Tony1_chang
B				
Date: Wednesday, April 10, 2019			Sheet	29 of 102

Only 3V Torlence

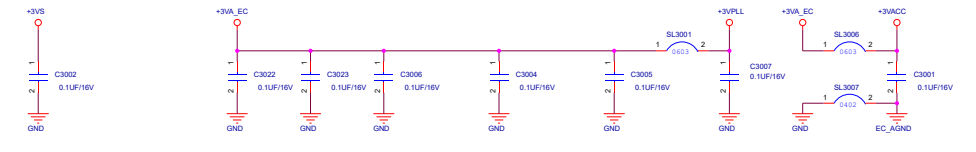
```
GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]
```

Can be adjusted to
Open-Drain for port:

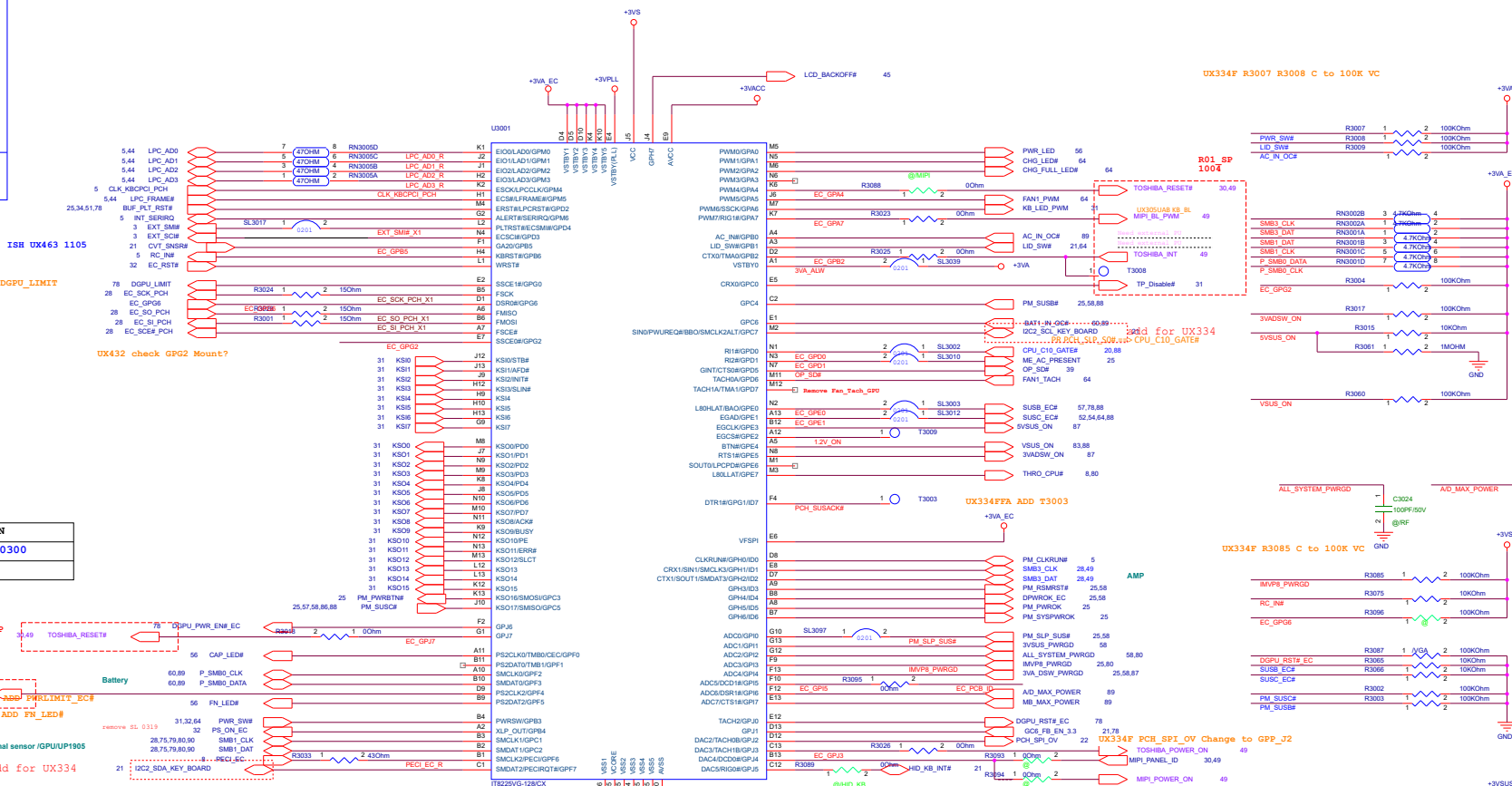
GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

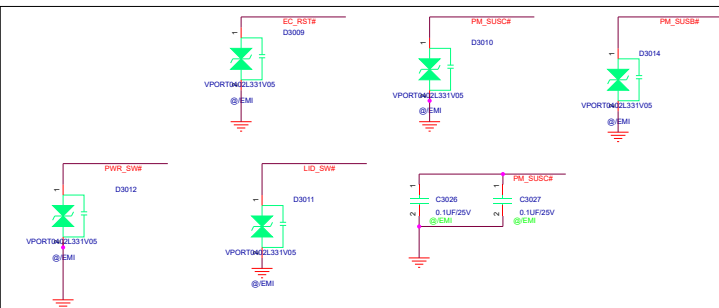
Power



UX431 Delete +3VA_EC C3022 10UF C3023 10UF




ITE Version	ASUS P/N
IT8225VG-128/CX	06037-00260300



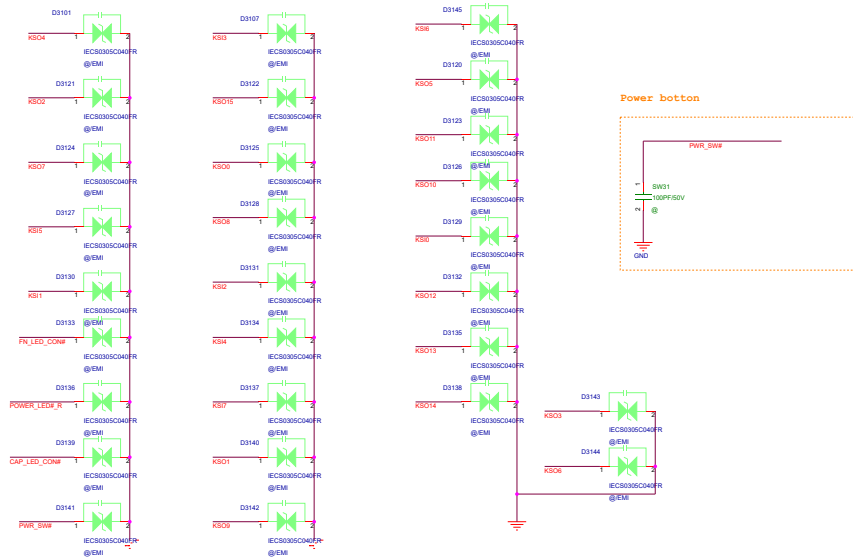
R3090	ID1 (Panel)		Screen Pad
14K	GND	0.4V	Tianma Panel
14K	18K	0.8V	BOE Panel
14K	NC	3.3V	No Screen Pad

<Variant Name>

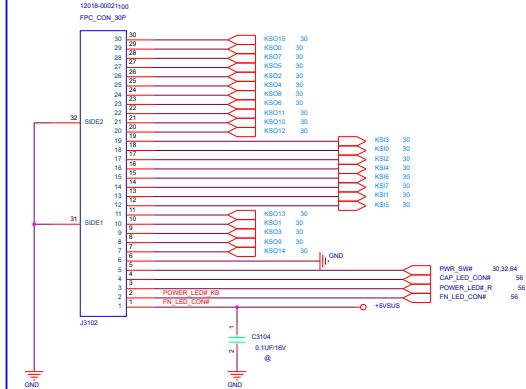
		Project Name	Rev
UX334F			R2
Title : CR_KBC_IT8521			
Size	Dept.:	Engineer:	
C	ASUS	Tony1_chang	
Date: Wednesday April 10, 2019	Sheet	30	of 102

	Rev
--	-----

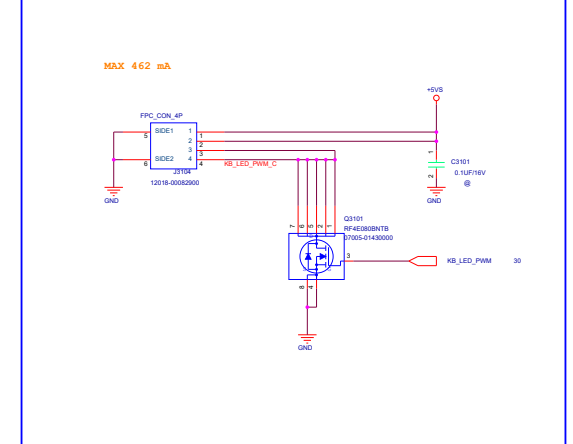
62



Keyboard_CON.



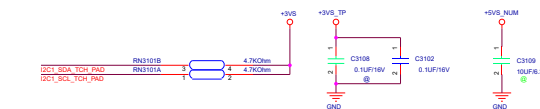
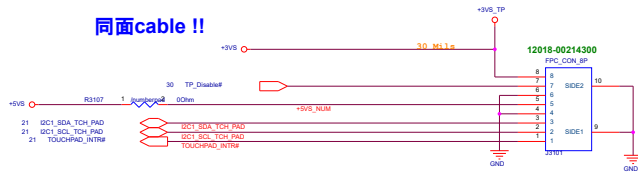
BL_CON.



Touch Pad & FP

Finger Printer (USB)

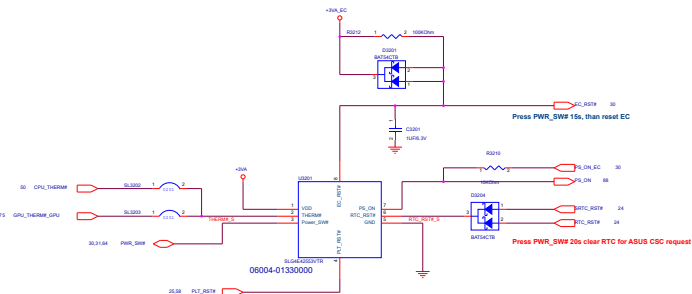
同面cable !!



UX432 Change J3101 PIN2 Change to TP_Disable# connect to EC GPC0 P30 P31

TP PIN#	Assignment
1	INT
2	I2C SCL
3	I2C SDA
4	GND
5	DM Key
6	X
7	Report_En
8	TP VDD

<Variant Name>



*Default Name

ASUS		Project Name	Rev
UX334F			R0.0
Title : RST_Reset Circuit			
Size	Dept.: ASUS	Engineer: Tony1_chang	
Date: Wednesday, April 10, 2019	Sheet	32	of 102



Project Name

UX334F

Rev

R2.0

Title : **LAN-CLARKVILLE**

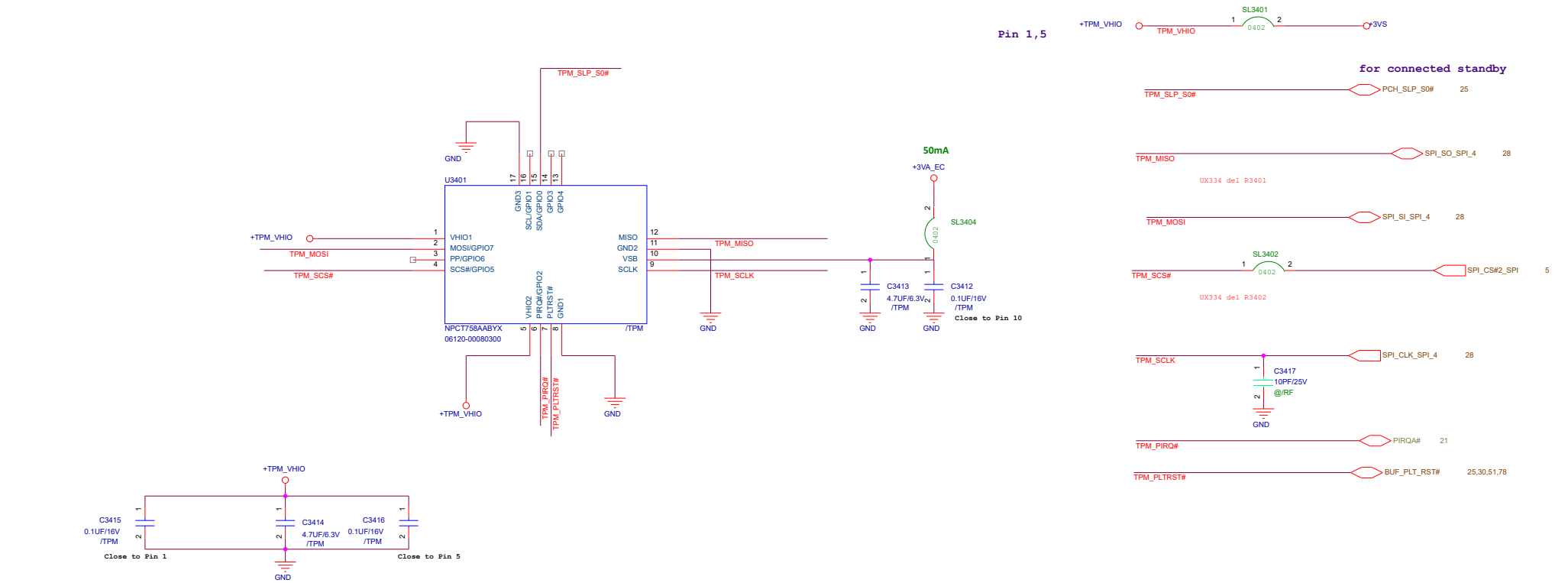
Size

A

Dept.: **ASUSTeK COMPUTER INC.** **Engineer:** **Tony1_chang**

Date: **Wednesday, April 10, 2019**

Sheet **33** of **100**




06120-00080000 TPM NPCT750AAAAX QFN32 NUVOTON TPM 2.0 SPI F/W:7.2.0.1

	Mount	Un-Mount
NPCT750A (SPI)	TPM	

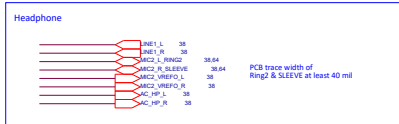
BUSPOWERZ

1 PD port solution can only PD 100K 0215

		Project Name UX334F		Rev R2.0
Title : PDC_TPS65982 & Type C conn				
Size C	Dept.: RD3-SYS2-EE2		Engineer:	Tony1_chang
Date: Wednesday, April 10, 2019			Sheet	38 of 102




UX432 C3641 C3608 C3637 C3606 Change to 4.7UF



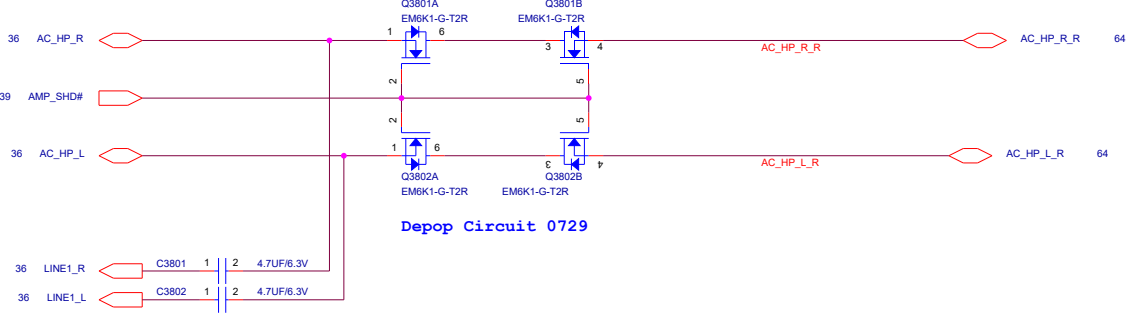
MC2_L_RING2	38.64	PCB trace width of Ring2 and SLEEVE at least 40 m
MC2_R_SLEEVE	38.64	
MC2_VREF0_L	38	
MC2_VREF0_R	38	

UX390 change to AZ2115-05F 1229

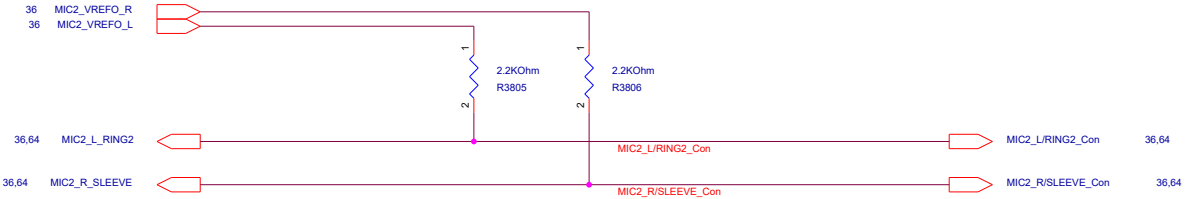
<Variant Name>

		Project Name UX334F		Rev R2.0
Title : AUD_				
Size A	Dept.: ASUSTeK COMPUTER INC. R&D Engineer: Tony1_chang			
Date: Wednesday, April 10, 2019			Sheet	37 of 100

20 mils



10 mils



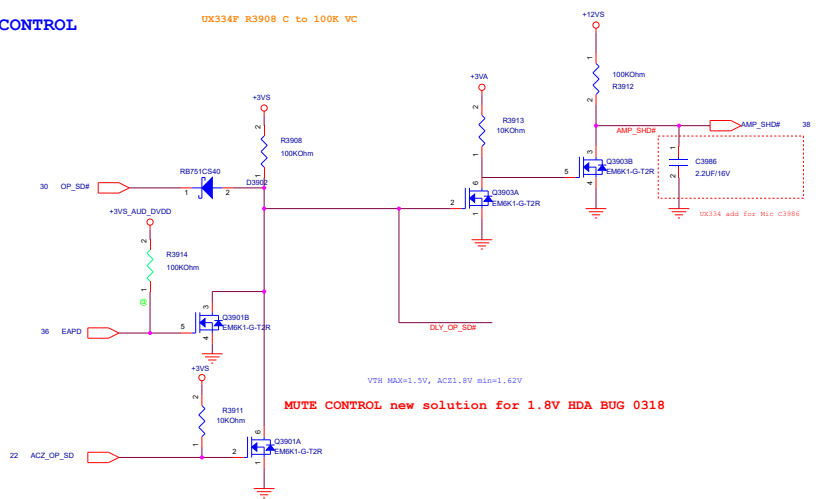
40 mils

UX432 Del @EMI @C3803 @C3804 @C3805 100PF



MUTE CONTROL

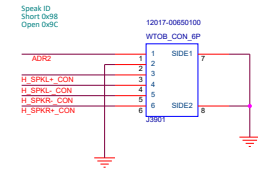
UX334F R3908 C to 100K VC



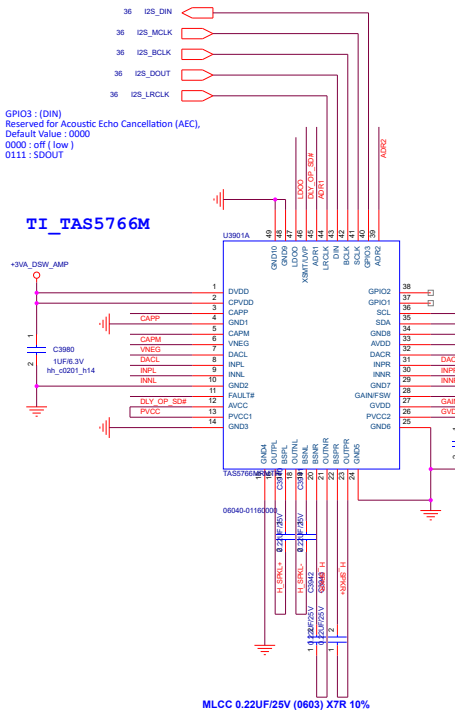
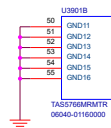
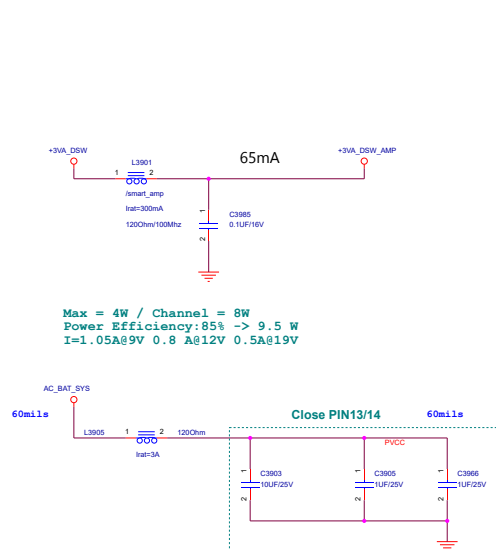
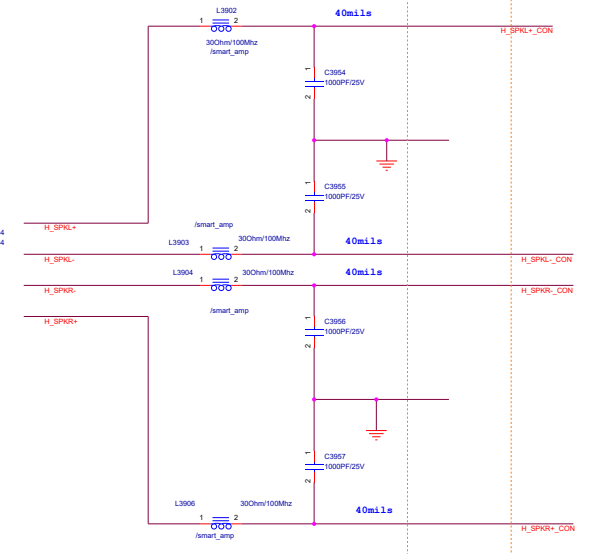
I2C Slave Address:
1001 100x = 98 & 1001 110x = 9C
0X98 (ADR2=0/ADR1=0)
0X9C (ADR2=1/ADR1=0)



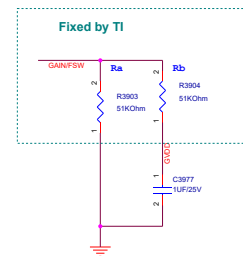
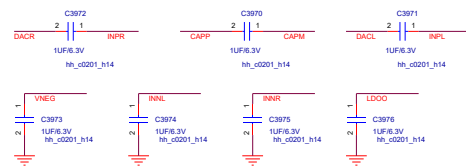
INTERNAL SPK Conn.
Max = 4W / Channel
I = 0.7 A (@Speaker : 8 Ohm)
SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 60mils




UX334 delete Snubber for EMI



MLCC 0.22UF/25V (0603) X7R 10%




	Project Name UX334F	Rev R2.0
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Title :	SDIO_CR
---------	----------------

Size A	Dept.: ASUSTeK COMPUTER INC. NB6	Engineer: Tony1_chang
---------------	----------------------------------	------------------------------

Date: Wednesday, April 10, 2019	Sheet 40 of 100
---------------------------------	-----------------

		Project Name		Rev
		UX334F		R2.0
Title : CB-****				
Size	Dept.:		Engineer:	
C	ASUS			Tony1_chang
Date: Wednesday, April 10, 2019			Sheet	41 of 102



Project Name

UX334F

<Variant Name>

Rev

R2.0

Title :

Size

A

Dept.:

ASUSTeK COMPUTER INC

Engineer:

Tony1_chang


Date: Wednesday, April 10, 2019

Sheet

42

of

100

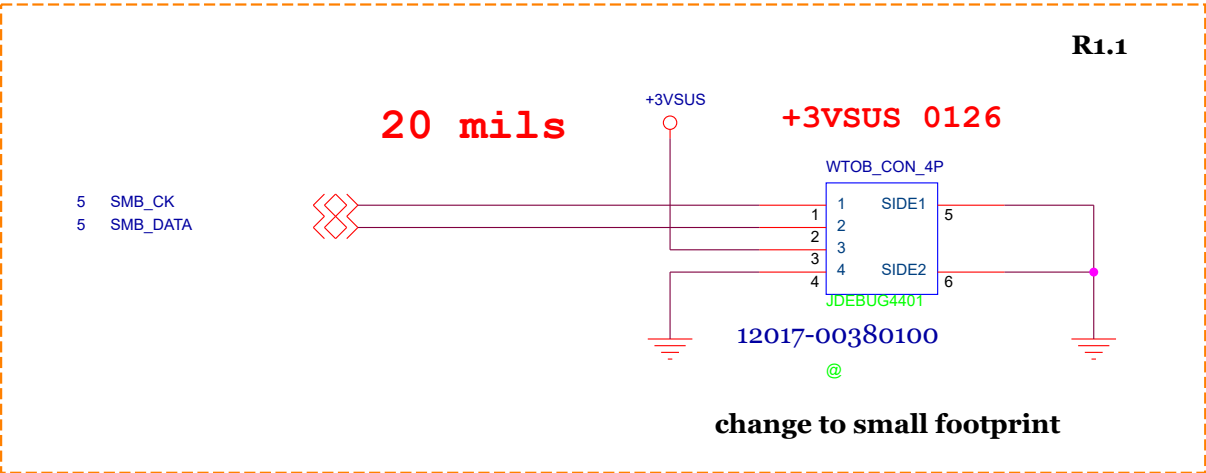
	Project Name UX334F	Rev R2.0
---	-------------------------------	-----------------

Title : CB-****

Size A	Dept.: ASUSTeK COMPUTER INC. Engineer: Tony1_chang
---------------	---

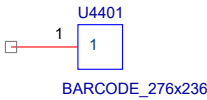
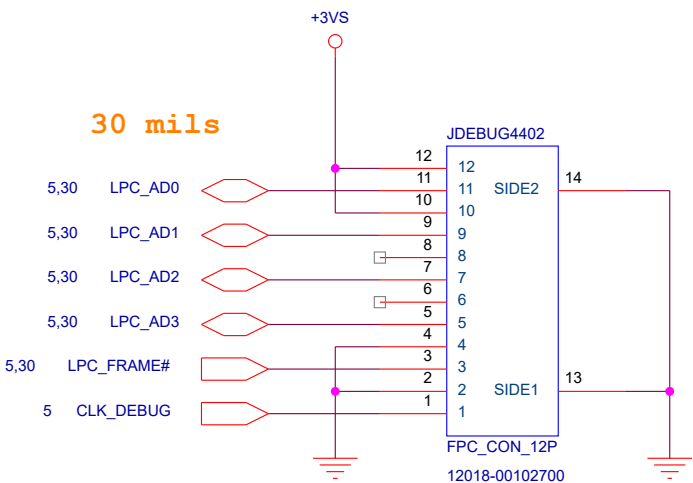
Date: Wednesday, April 10, 2019	Sheet 43 of 100
---------------------------------	-----------------

New Design Debug Port



LPC Debug Port

Follow UX370UAR 12018-00102300



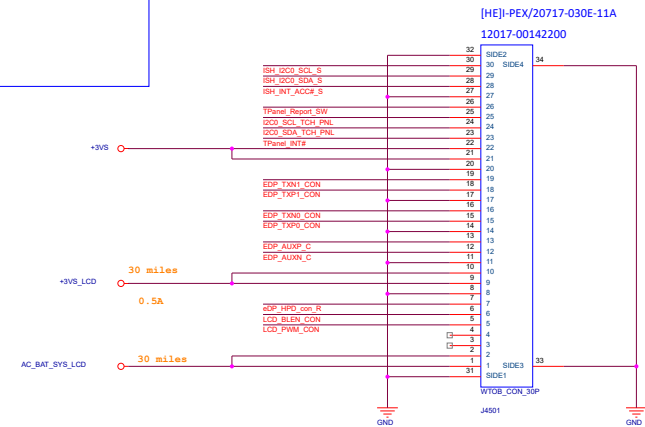
<Variant Name>

ASUS		Project Name	Rev
		UX334F	R2.0
Title : BUG_Debug			
Size A4	Dept.: ASUSTeK COMPUTER INC.	Engineer: Tony1_chang	
Date: Wednesday, April 10, 2019	Sheet	44	of 100

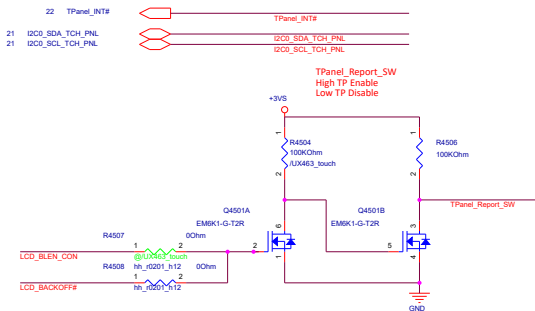
UX334 +3VS_LCD Discharge change to 120ohm



LED Control Signals



FOLLOW T303
power 3VS



21 ISH_INT_ACCE_S

21 ISH_DCO_SCL_S

21 ISH_DCO_SDA_S

SL4501 1 2

SL4504 1 2

0201

+3VS


BMA255/BMA253

0011000xb (18h) SDO = 0 (Default)

0011001xb (19h) SDO = 1 (alternative)

21 ISH_INT_ACCE28_S

<Variant Name>

		Project Name UX334F		Rev R2.0
Title : CRT_D-Sub				
Size A	Dept.: ASUSTeK COMPUTER INC. NB4 Engineer: Tony1_chang			
Date: Wednesday, April 10, 2019			Sheet	46 of 100

<Variant Name>



Project Name

UX334F

Rev

R2.0

Title : **Display Port**

Size

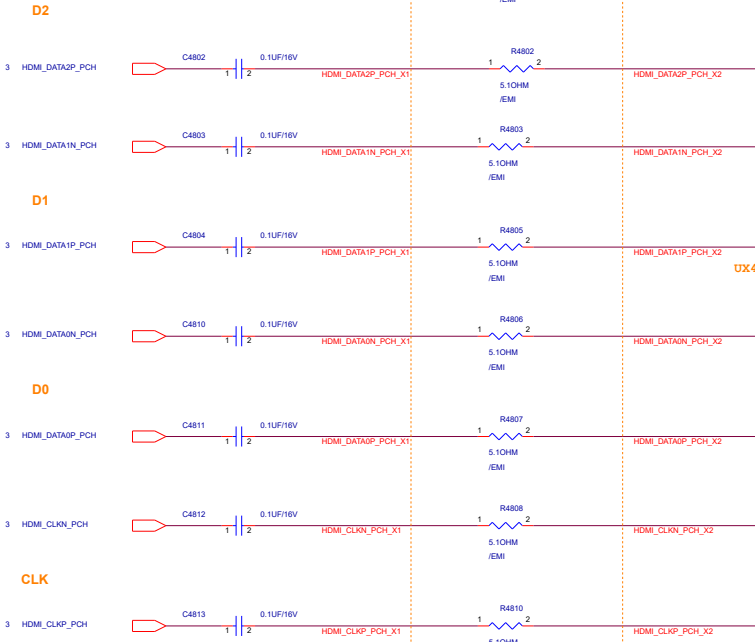
A

Dept.: **ASUSTeK COMPUTER INC. NSA** **Engineer:** **Tony1_chang**

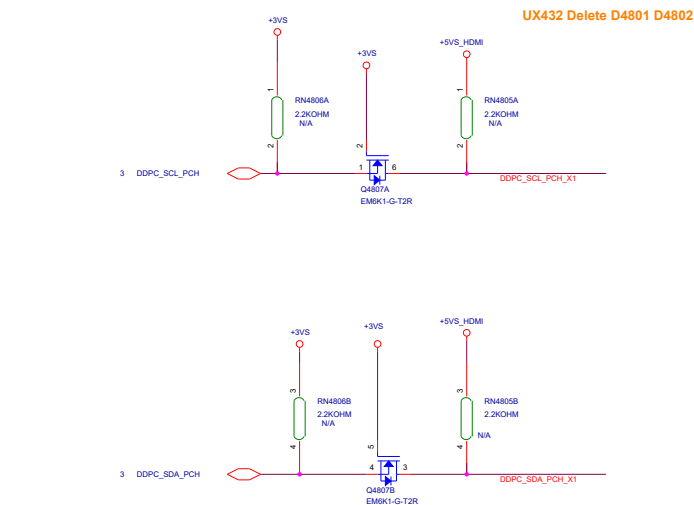
Date: **Wednesday, April 10, 2019**

Sheet **47** **of** **100**

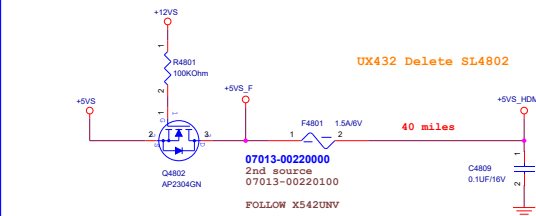
HDMI Signals



HDMI DDC Level-shifter

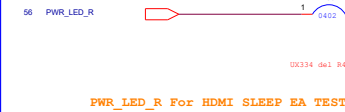


HDMI Power

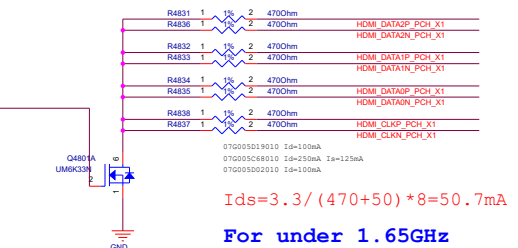


HDMI Cost-reduced Level shiter

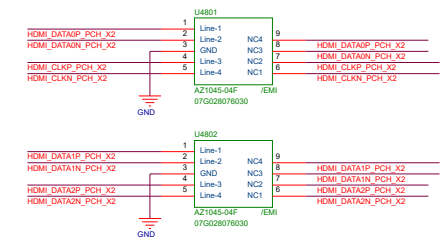
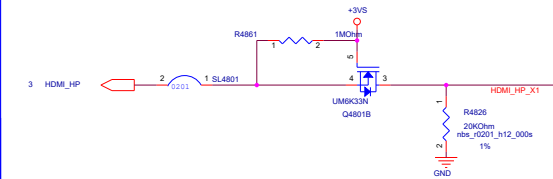
Delete KB_PWR_LED_EN GPP_P15 @R4810 @R5603 P21 P48 P56



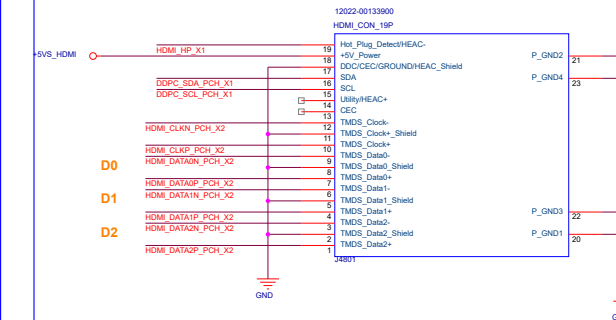
HDMI 1.4 WHL PDG Change to 470 ohm

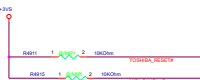
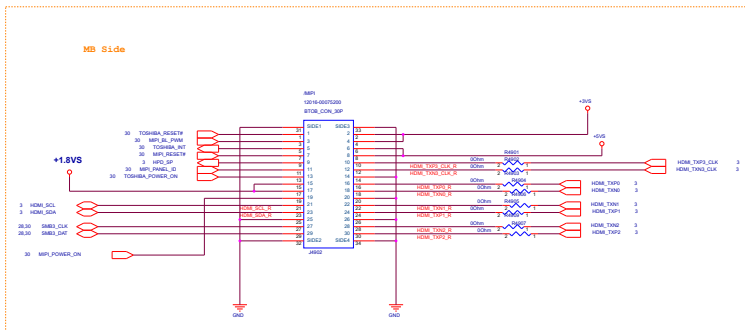


HDMI HPD



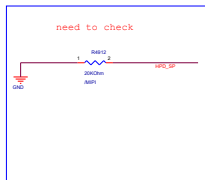
HDMI CON.





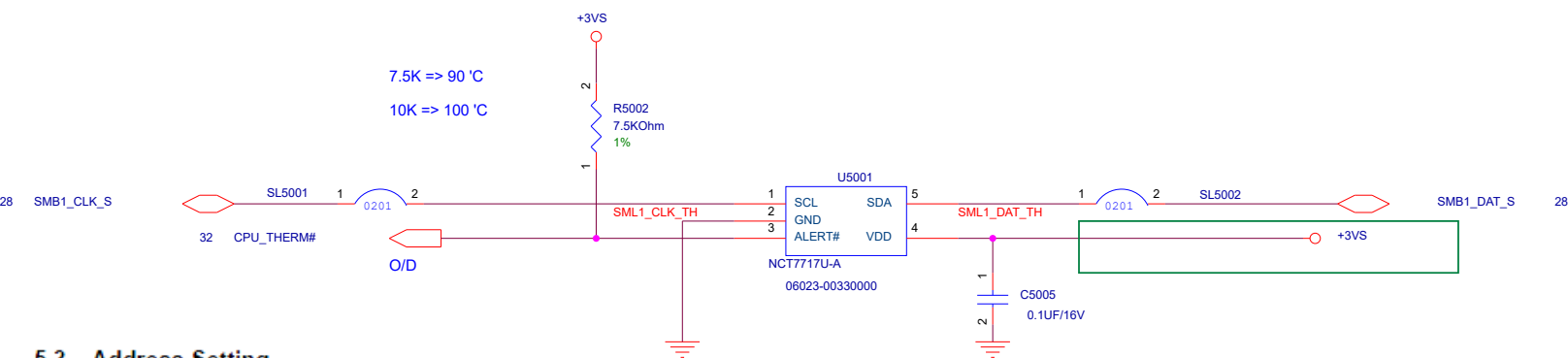
I2C Slave address

UX334 delete



UX334 move to IO_Board

CPU Thermal Sensor



5.3 Address Setting

NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

5.6 ALERT# point hardware power-on setting (TBD)

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

PULL-UP RESISTOR		TEMPERATURE (°C)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

<Variant Name>

SSD CONN.

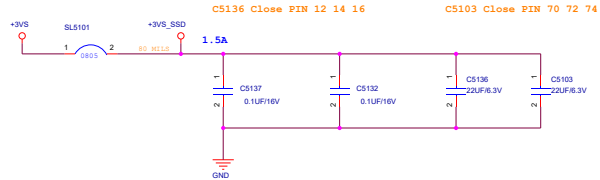
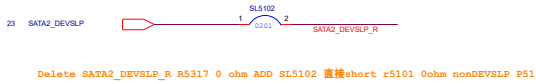


Table 36-7. SATA / PCI Express® Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA Only	PCI Express® Gen 2/ SATA	PCI Express® Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

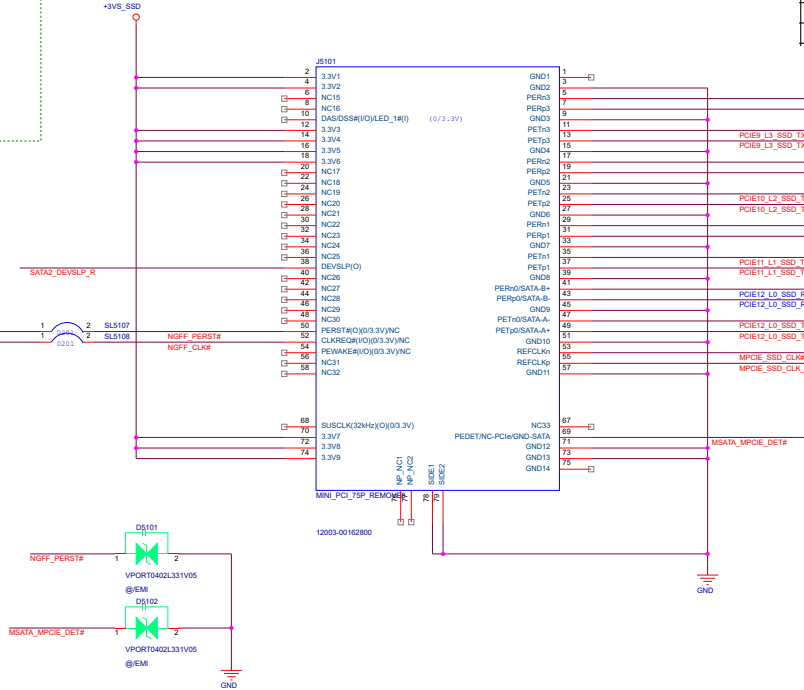
SATA DEVSLP.



PCIe Wake-up.

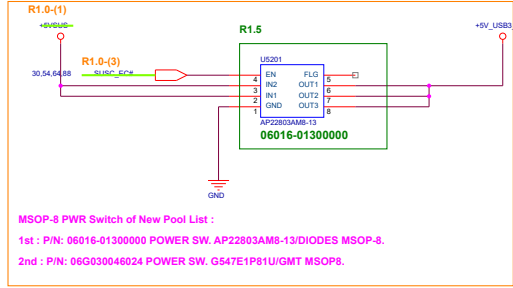


UX432 Delete @R5103 @C5199 R5105 MSATA_MPCIE_DET# (UX370)
PULL HIGH PCH Side R2302

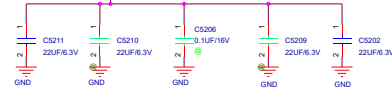


BOM

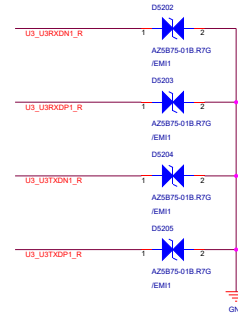
R1.0



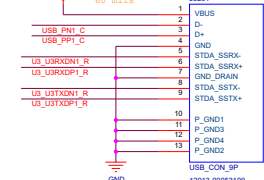
+5V_USB3_1



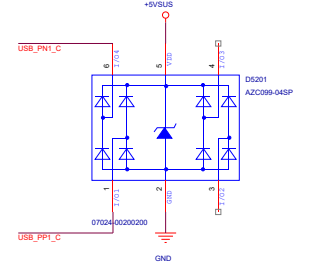
USB3.0 ESD-Protection



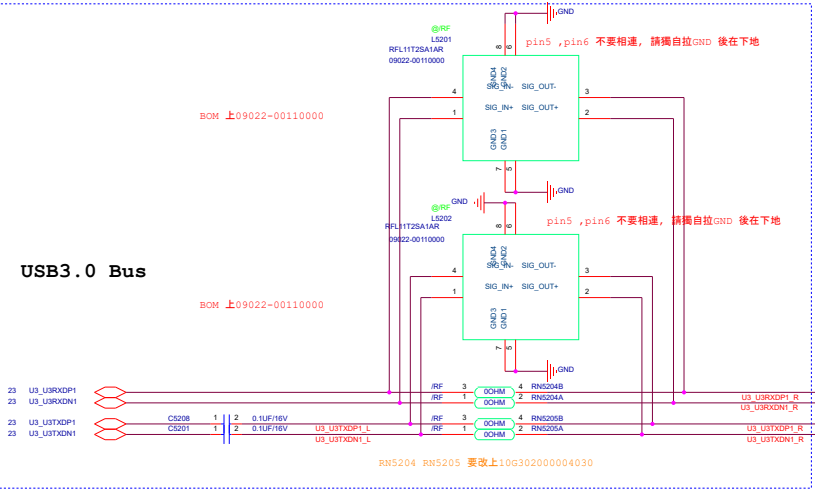
+5V_USB3_1



USB2.0 ESD-Protection



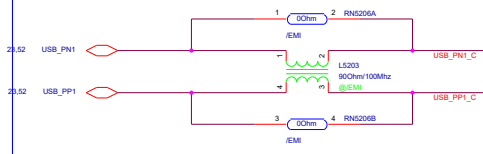
USB3.0 Bus



23.52 USB_PP1

23.52 USB_PN1

USB 2.0 Common choke EMI-Protection



<-Variant Name>



Project Name

UX334F

Rev

R2.0

Title : **RTS544x**

Size

C

Dept.: **ASUSTeK COMPUTER INC. NB4**

Engineer:

Tony1_chang

Date: **Wednesday, April 10, 2019**

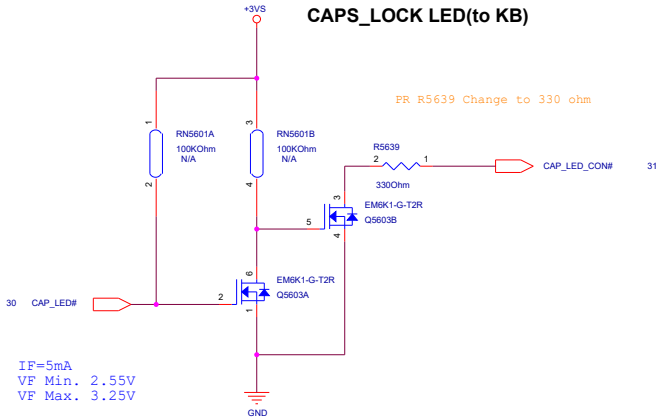
Sheet

55

of

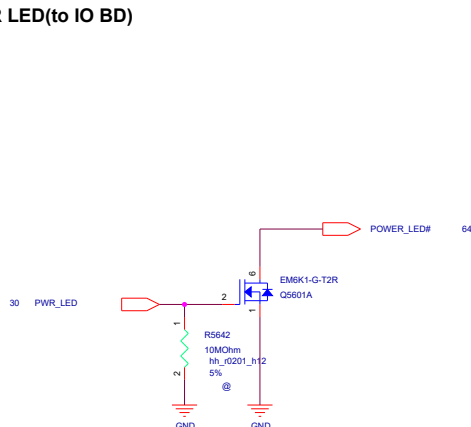
102

CAPS_LOCK LED(to KB)

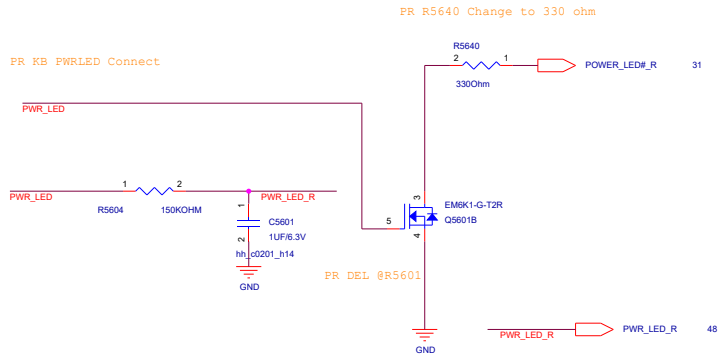


IF=5mA
VF Min. 2.55V
VF Max. 3.25V

PWR LED(to IO BD)

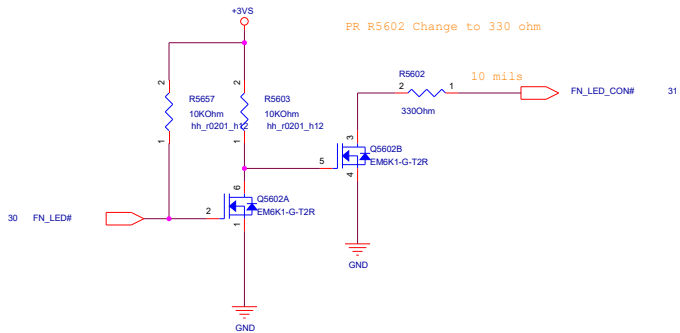


PWR LED(to KB)



FN LED

UX391UA FN LED

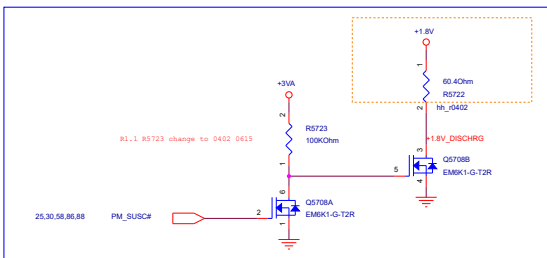


Charger LED

Change Charger LED 07014-00190300 (1015)

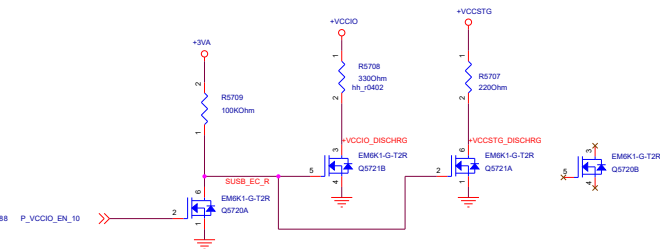
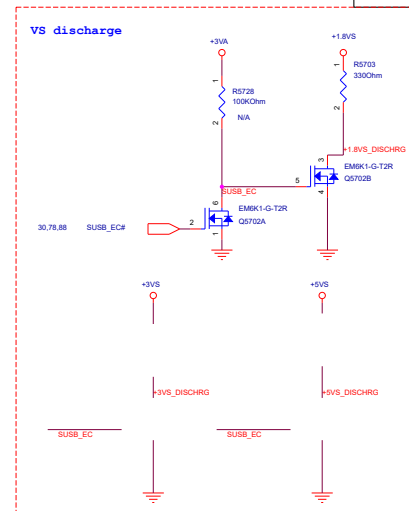
WHITE
IF = 5.6~6.5mA
VF Typ. = 2.85V
VF Max. = 3.15V

ORANGE
IF = 7.88~9.1mA
VF Typ. = 2.0V
VF Max. = 2.4V



+1.2V Change to +1.8V

DEL +1.05VSUS Discharge



<Variant Name>

ASUS Project Name
UX334F

Rev
 R2.0

Title : **DSG_Discharge**

Size Dept: **ASUSTek COMPUTER INC.** Engineer: **Tony1_chang**

Date: Wednesday, April 10, 2019 Sheet 57 of 100

VCCST_PWRGD for PCH

UX432 R1.1 Delete @D5804

UX432 Delete R5802 直接short

ALL_SYSTEM_PWRGD

R1.1 C5804==>R5807 UX432FD
CHECK

<Variant Name>

ASUS UX334F

Project Name

Title : PRO_Protect

Size

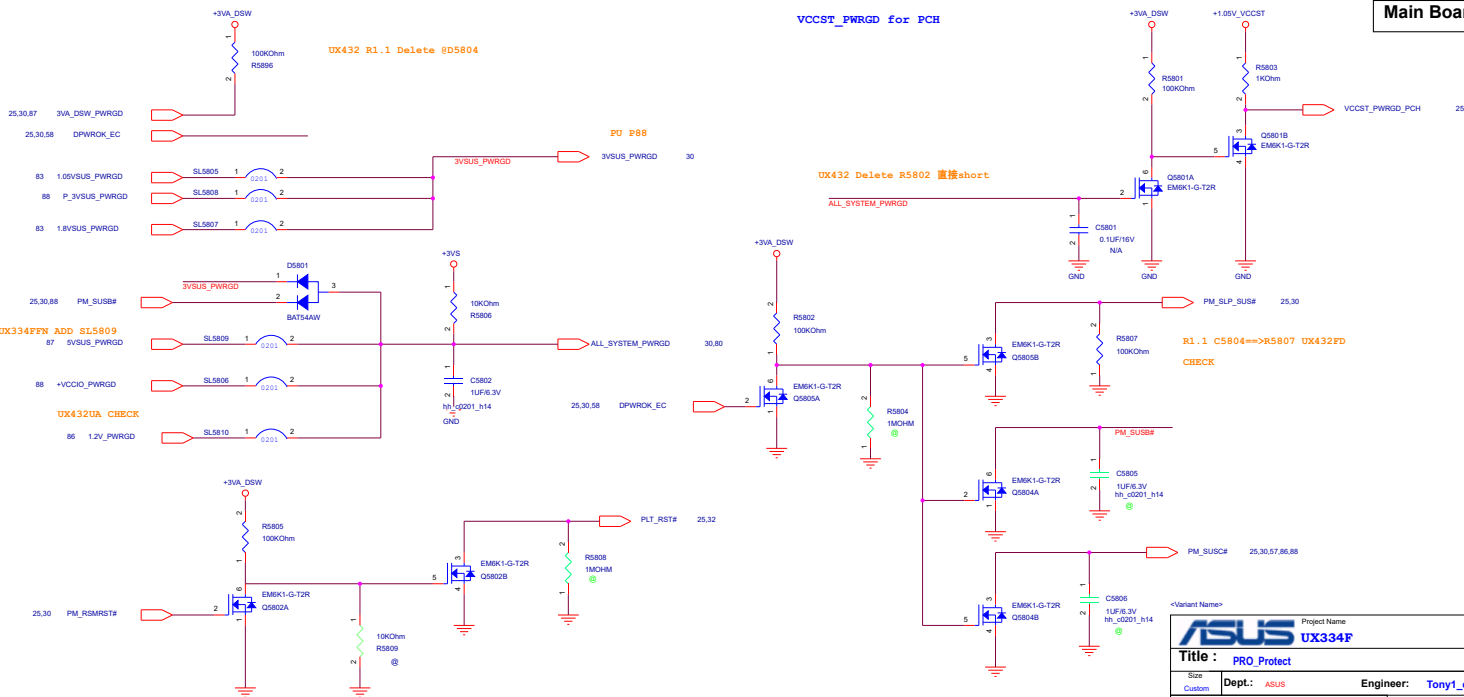
Custom

Dept.: ASUS

Engineer: Tony1_chang

Date: Wednesday, April 10, 2019

Sheet 58 of 102

Rev
R2.0



Project Name:

UX334F

Rev:

E3.0

Title : NGFF_WMAN

Size:

A

Dept.: ASUS/TAIwan COMPUTER INC. Engineer: Tony1_chang

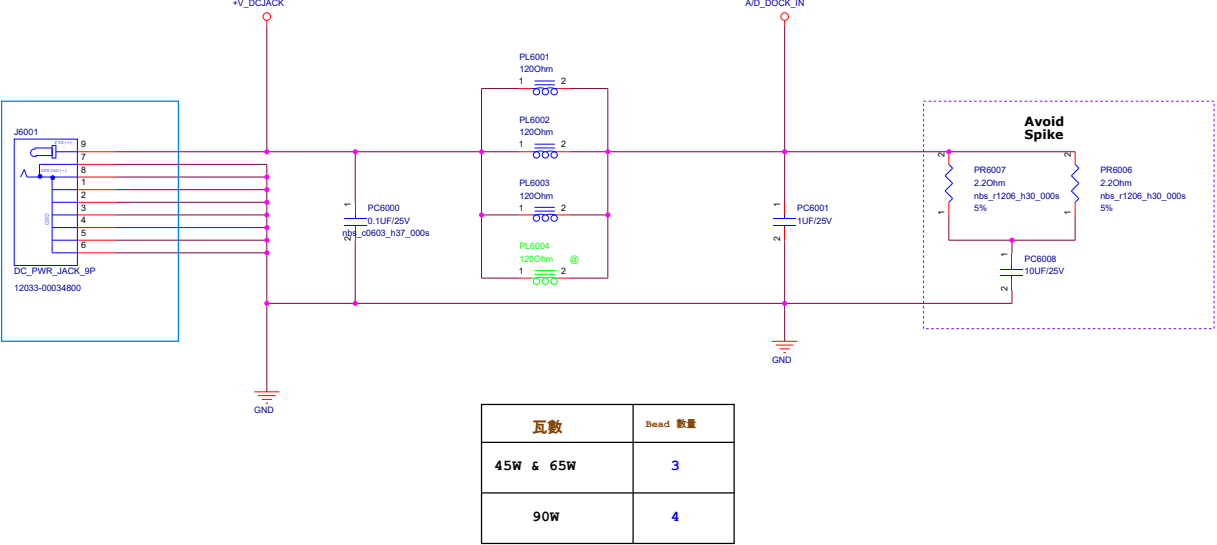
Date: Wednesday, April 10, 2013

Sheet

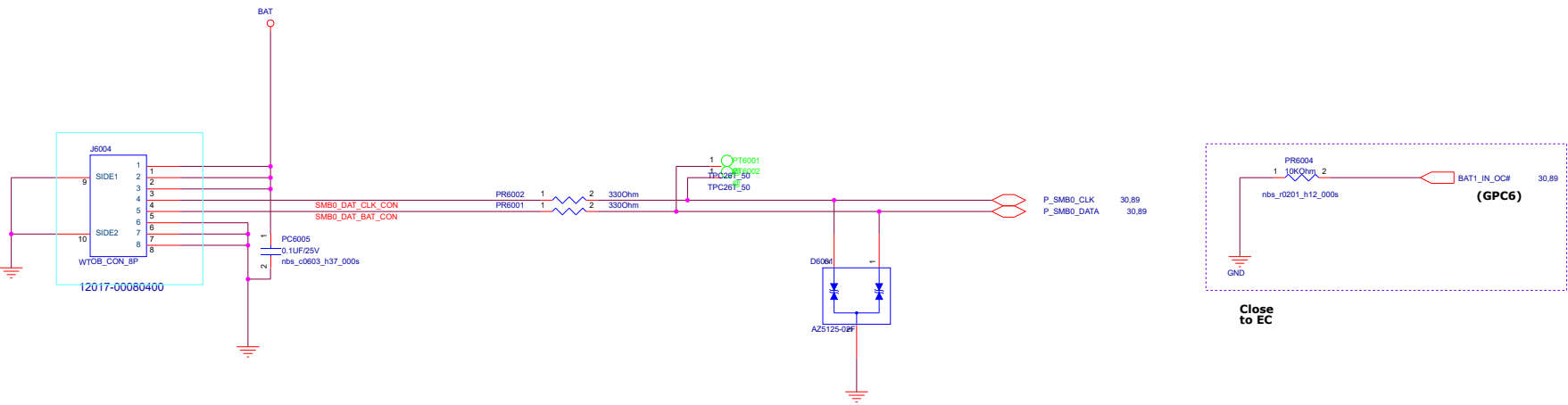
39

of

100



Battery Connector



<Variant Name>

	Project Name: UX334F	Page: P2.0
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Title : MB to I/O_CONN.

Spec 	Dept.: ASUSTEK COMPUTER INC. Engineer: Tony1_chang
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Date: Wednesday, April 10, 2013	Sheet 61 of 100
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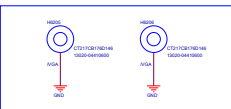
CPU

13020-04410600

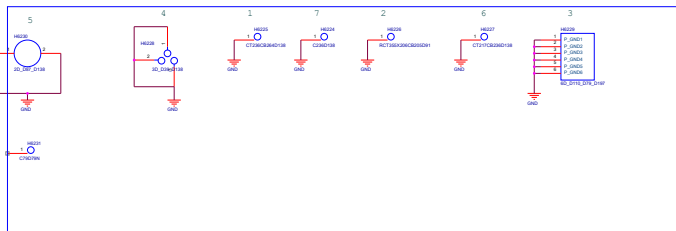


GPU

13020-04410600



ME Hole



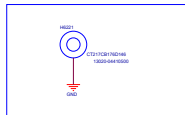
B TO B

13020-04410400

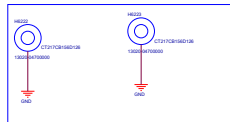


SSD NUT

13020-04410500



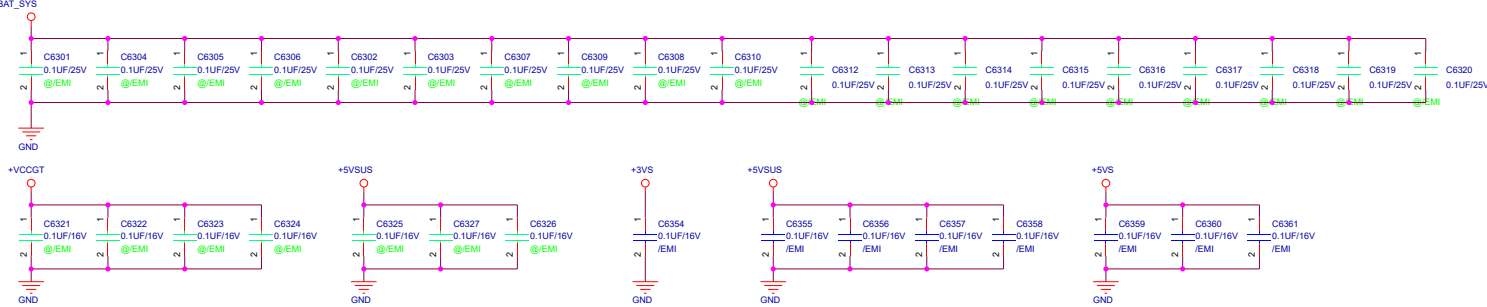
B TO B



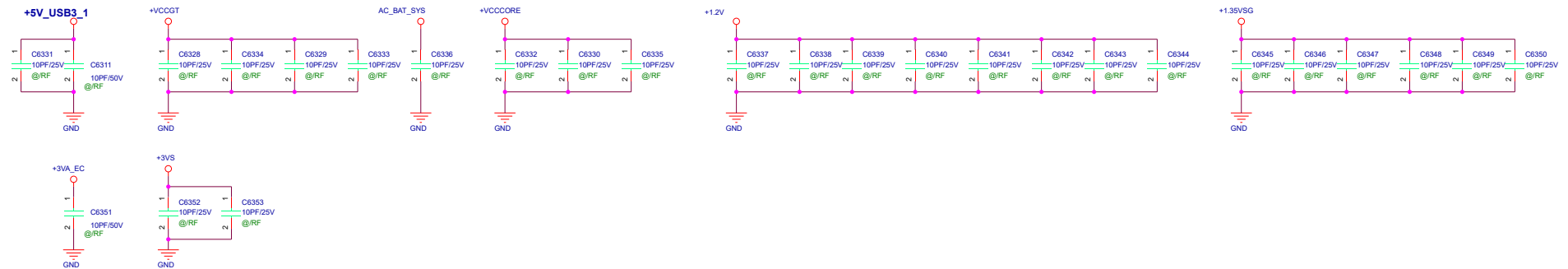
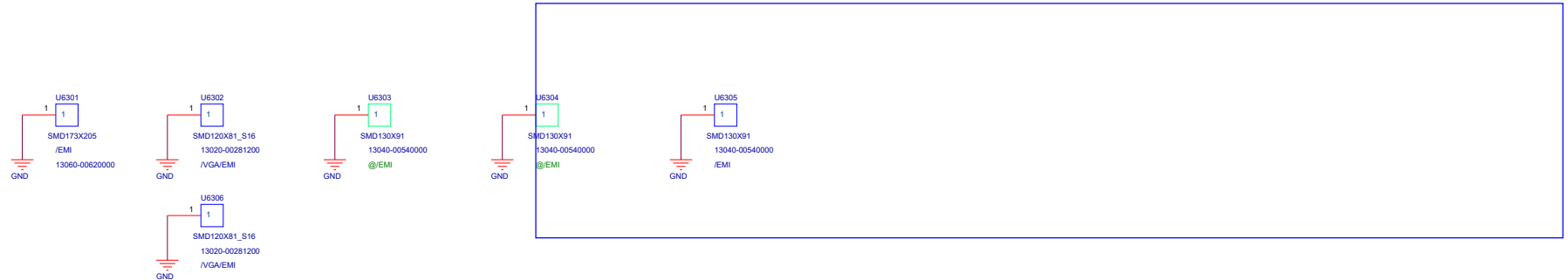
UX334 del RF ANTENNA Coaxial cable Clip

<Default Name>

Project Name		Rev
ASUS UX334F		R2.0
Title : view		
Drawn	Dept.: ASUS WARE COMPUTER INC.	Engineer: Tony1_chang
Date: Wednesday, April 16, 2015	Sheet: 62	of 100




EMI



<Variant Name>

ASUS UX334F		Project Name	Rev
Title : EMI RF reserve CAP			R2.0
Size Custom	Dept.: ASUS	Engineer:	Tony1_chang
Date: Wednesday, April 10, 2019	Sheet	63	of 102


	Project Name UX334F	Rev R2.0
---	-------------------------------	-----------------

Title : ME_Conn & Skew Hole


Size C	Dept.: ASUSTeK COMPUTER INC. NB2EE1	Engineer: Tony1_chang
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Date: Wednesday, April 10, 2019	Sheet 65 of 102
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<Variant Name>

		Title : IO_BD-1	
ASUSTeK COMPUTER INC.		Engineer: Tony1_chang	
Size Custom	Project Name UX334F		Rev R2.0
Date: Wednesday, April 10, 2019		Sheet 66 of 102	

<Variant Name>

		Title : IO_BD-2(AU6465RB63)	
ASUSTeK COMPUTER INC.		Engineer: Tony1_chang	
Size	Project Name		Rev
Custom	UX334F		R2.0
Date: Wednesday, April 10, 2019		Sheet 67 of 102	



Project Name

UX334F

Rev

R2.0

Title : **USB3.0_PortA**


Size

A

Dept.: ASUSTeK COMPUTER INC. NB2EE1 **Engineer:**

Date: Wednesday, April 10, 2019

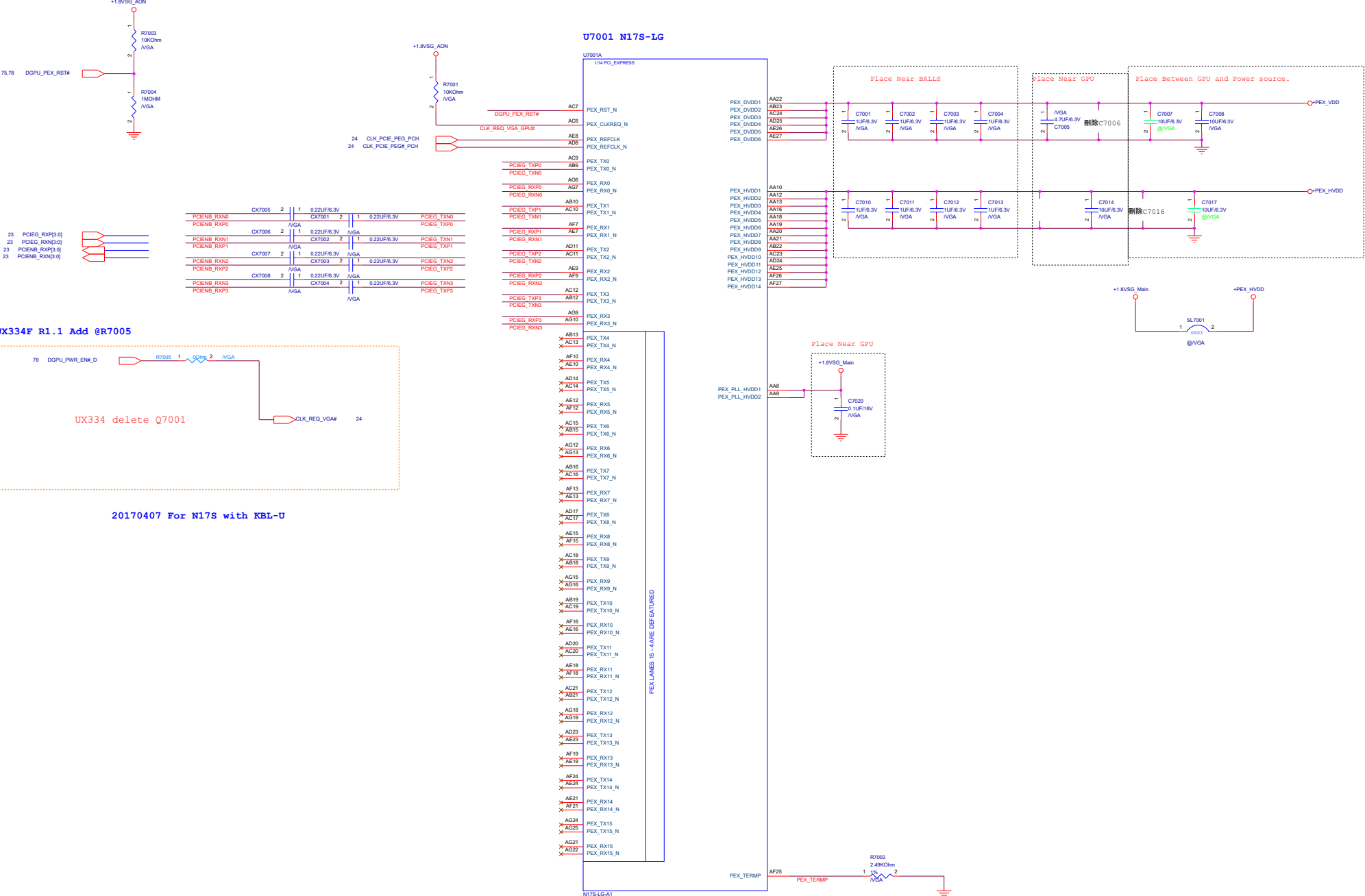
Sheet 68 of 100

	Project Name UX334F	Rev R2.0
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Title : MINICARD_Wlan & BT

Size A	Dept.: ASUSTeK COMPUTER INC. NB2EE1	Engineer: Tony1_chang
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Date: Wednesday, April 10, 2019	Sheet 69 of 100
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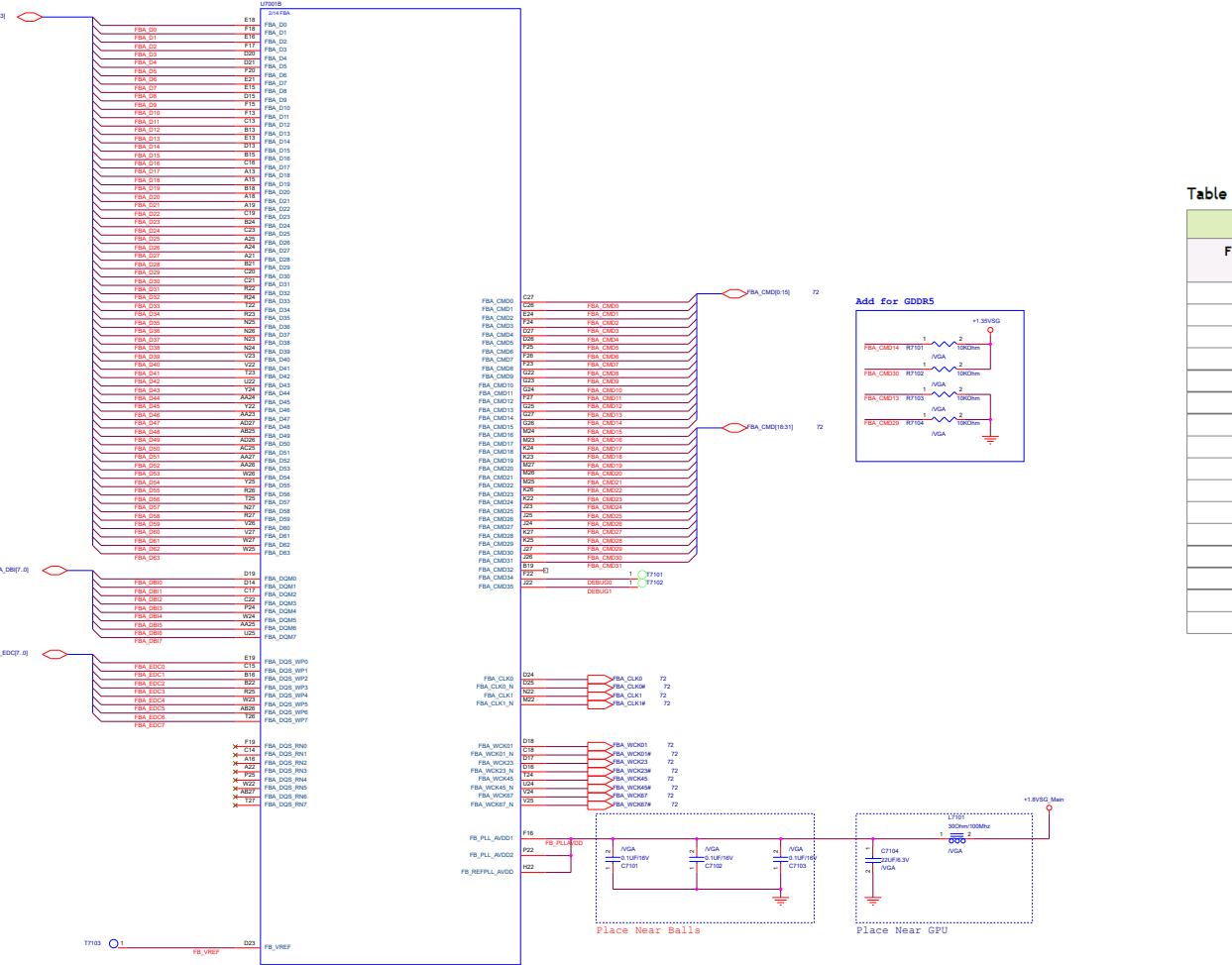


Table 9.5 GDDR5 Command Mapping (GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	AB1*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

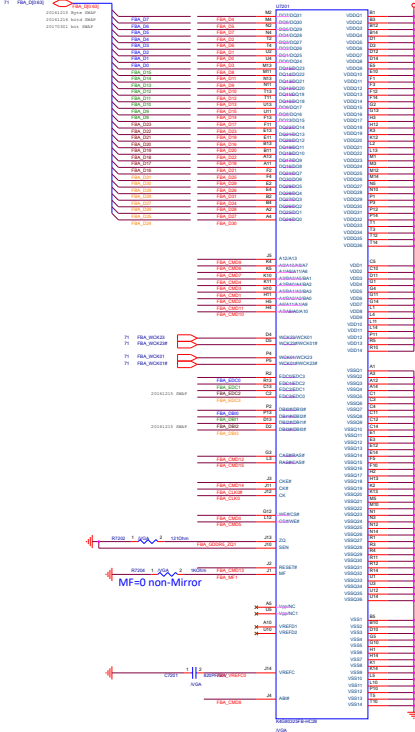
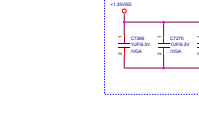
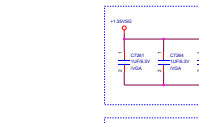
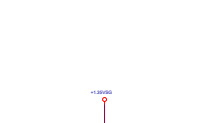
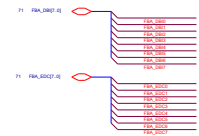
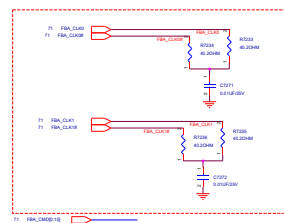
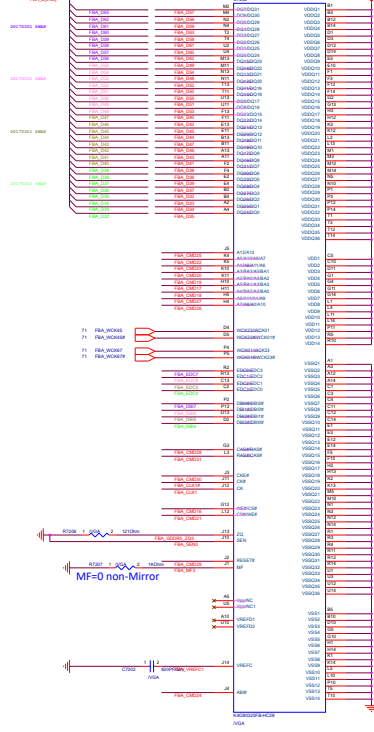
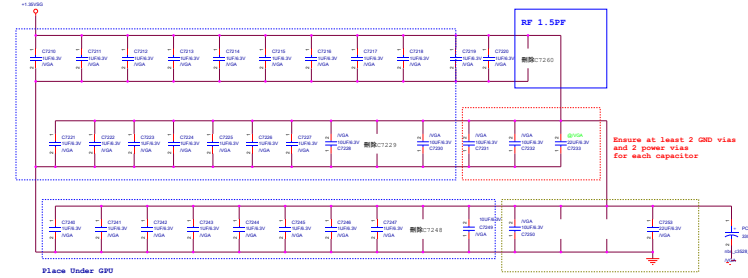


Table 9.5 GDDR5 Command Mapping (GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A9*
FBA_CMD8	FBA_CMD24	AB0
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*



Place Under DRAM

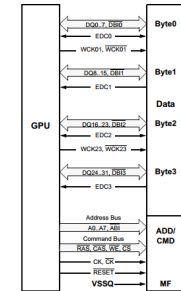


Place Under GPU

Place Near GPU

Ensure at least 2 0MD vils and 2 power vils for each capacitor

x32 Mode





Project Name

UX334F

Rev

R2.0

Title : **VGA_******

Size

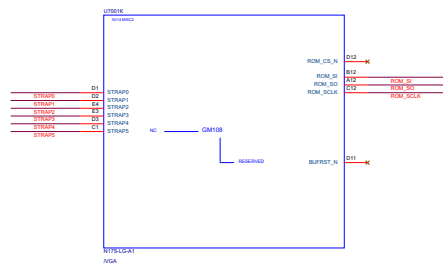
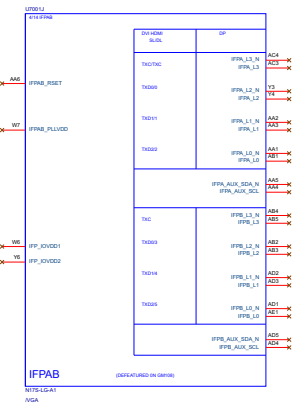
B

Dept.: **RD3_EE2**

Engineer: **Andy_Ceng**

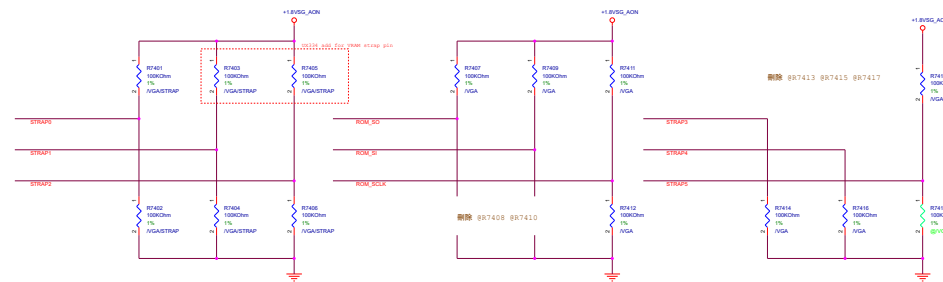
Date: **Wednesday, April 10, 2019**

Sheet **73** of **102**



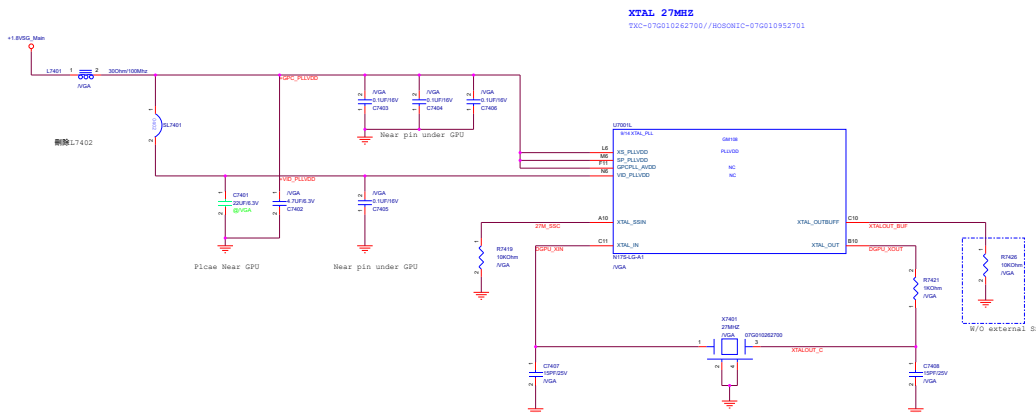
Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade
8 Gb	256Mx32	1.35V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps
			Micron	MT51J256M32HF-70A	A-die	0x1	7 Gbps

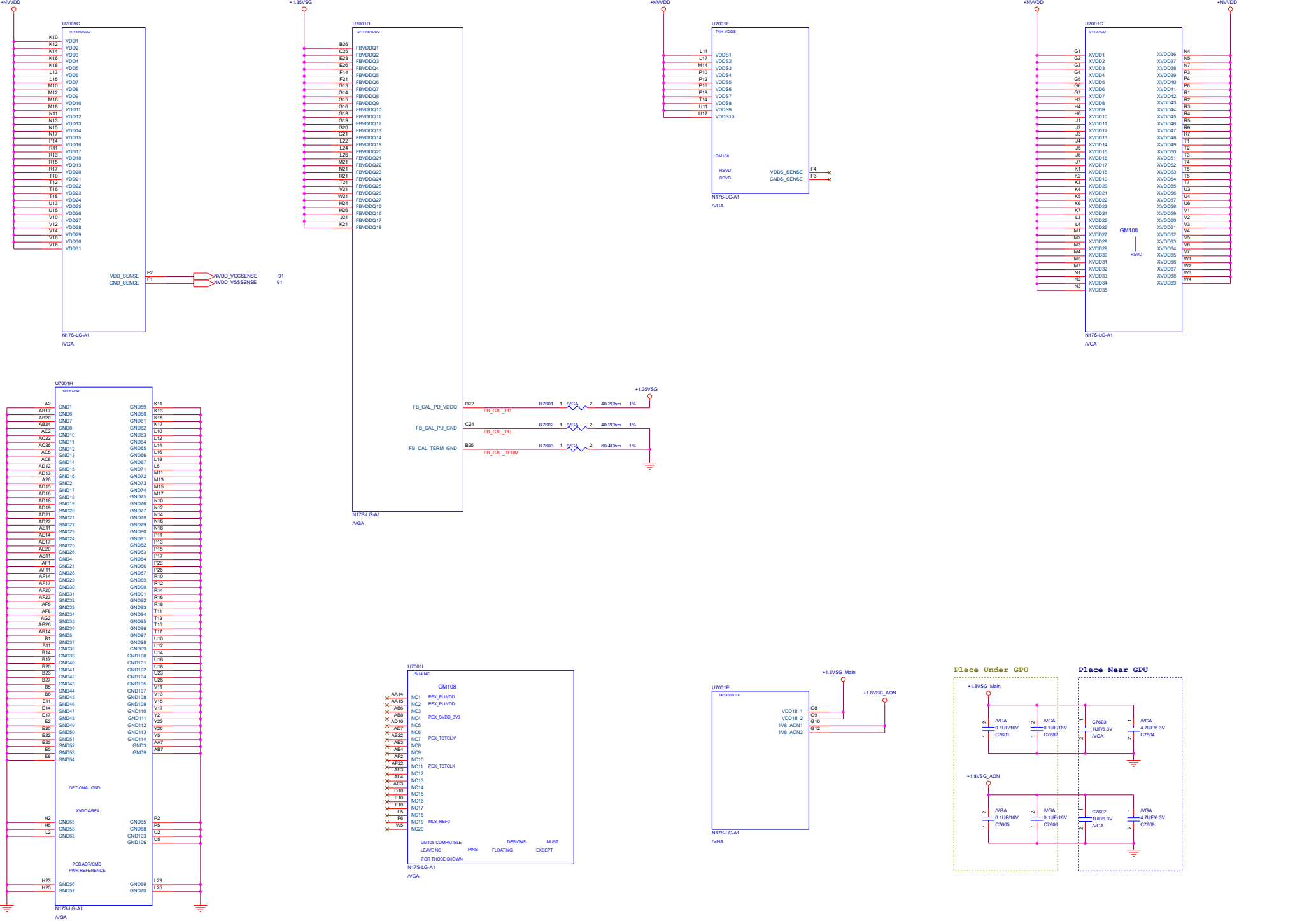


Row Index	Strap Pins see Note			Resulting SOR_XPOSED Enablements			
	ROM_SO	ROM_SI	ROM_CLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
0	H	H	M	disabled	disabled	disabled	disabled

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

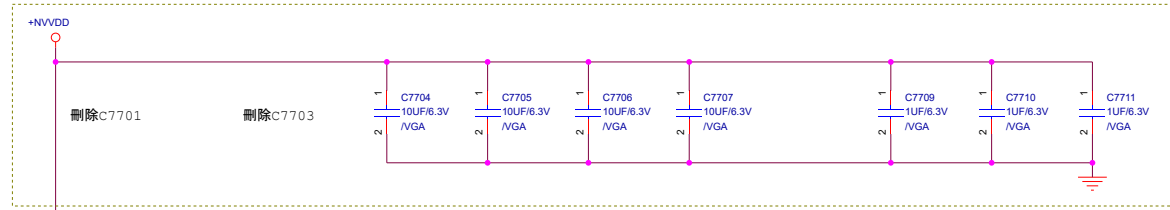


- **SMB_ALT_ADDR Enable:** This strap function allows an alternate SMBus address to be configured, so that graphics circuits with multiple GPUs can have separate SMBus connections for each GPU. In dual GPU configurations, use of the alternate address on one GPU (by setting this function to '1') avoids conflicts between the two GPUs on an SMBUS port. The "SMB_ALT_ADDR disabled" setting ('0') is correct for single-GPU graphics circuits. (see [Section 13.3.2.1](#) for the SMBus address.)
- **DEVID_SEL:** NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID defined for the GPU (via a function setting of '0'), and the alternate "re-brand" Device ID defined for the GPU (via a function setting of '1').
- **PCIE_CFG:** This function sets electrical characteristics of PCIe lanes, in particular signal amplitude (swing). A setting of '0' selects normal (full) signal swing. N17x graphics circuits should strap for this setting. (A setting of '1' designates reduced signal amplitude, available if special concerns require. Consult NVIDIA for guidance.)
- **VGA_DEVICE:** This strap function is used to report the graphics circuit either as a 3D device (class code 302, designated by a setting of '0' for this strap) or as a VGA device (class code 300, designated by a setting of '1') to the host system. The 3D Device (class code 302, strap=0) setting is correct for most MS-Hybrid notebook GeForce graphics circuits.

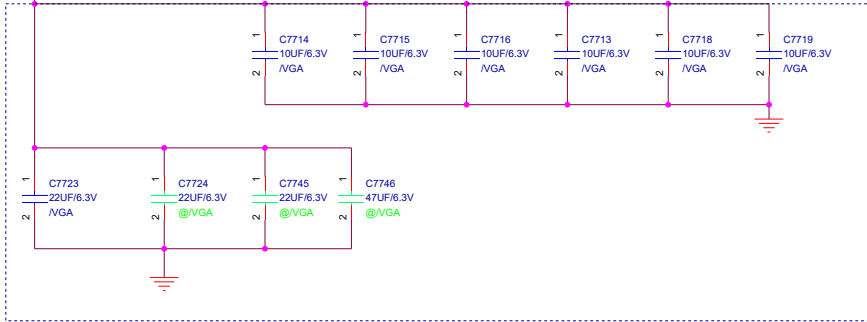


NVDD POWER AND DECOUPLING

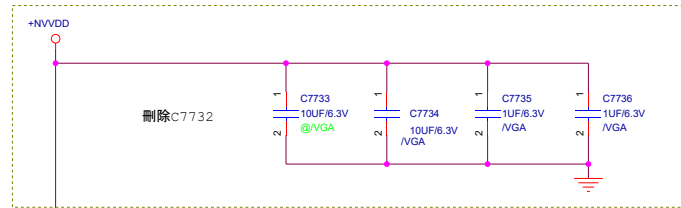
Place Under GPU



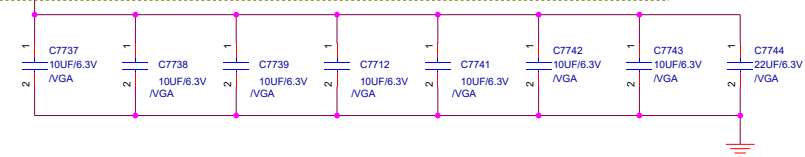
Place Near GPU



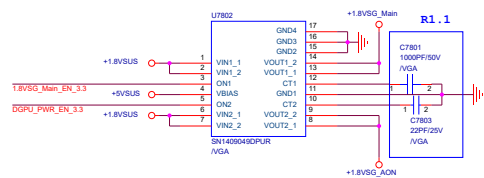
Place Under GPU



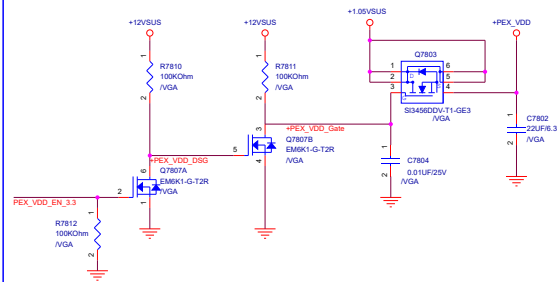
Place Near GPU



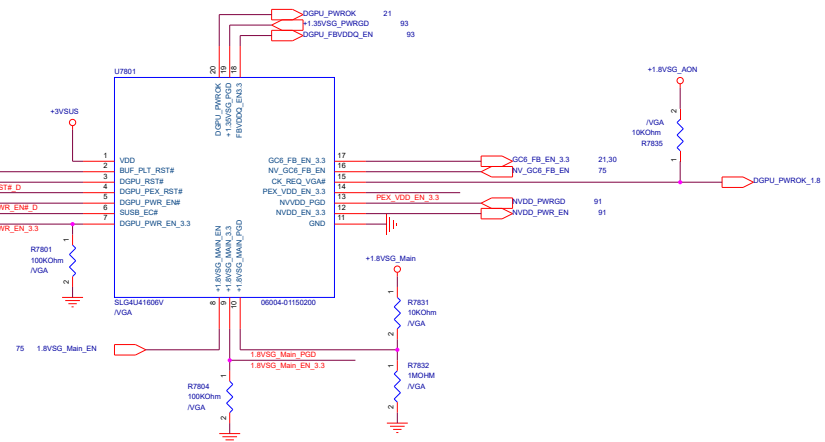
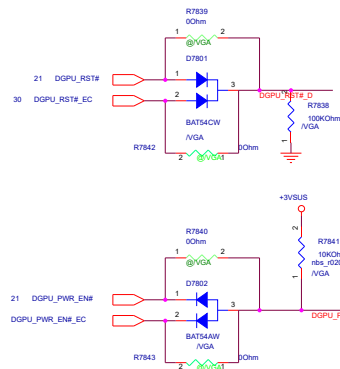
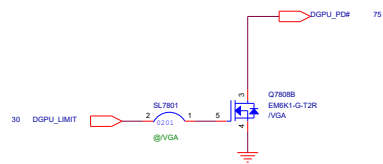
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+1.8VSG_Main



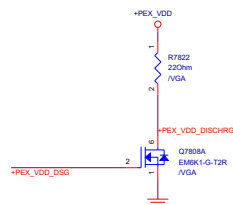
+PEX_VDD



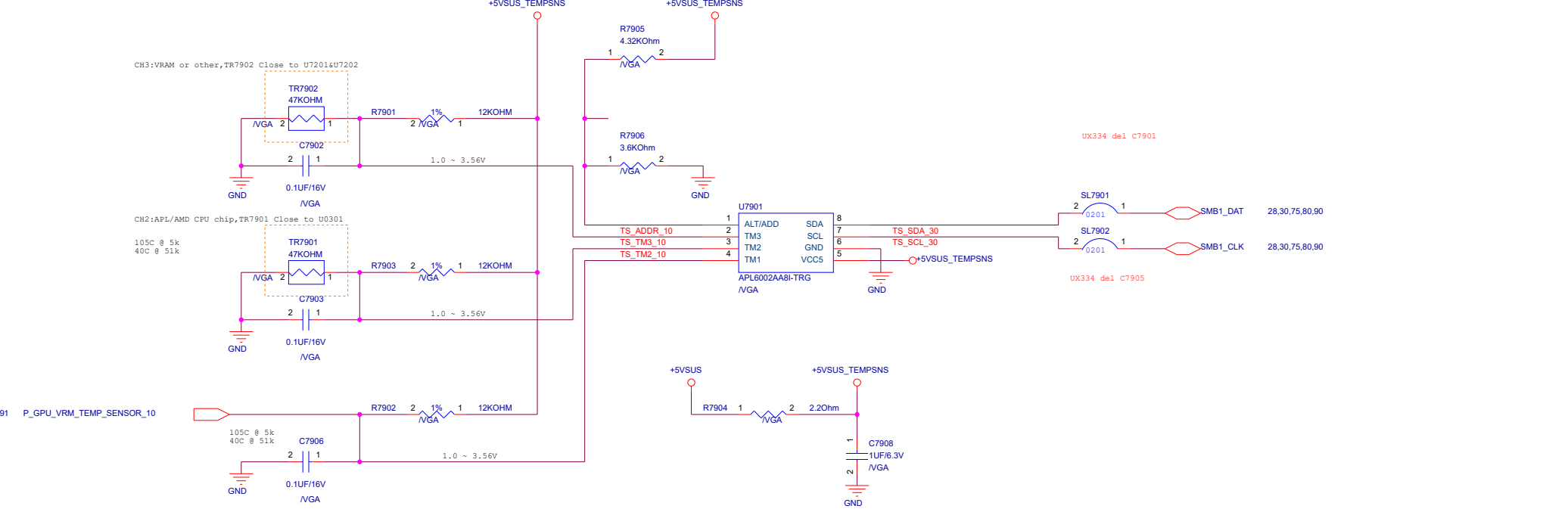
DGPU_PD#



Discharge



刪除SR測試用LED
R7813
LED7801
Q7810A

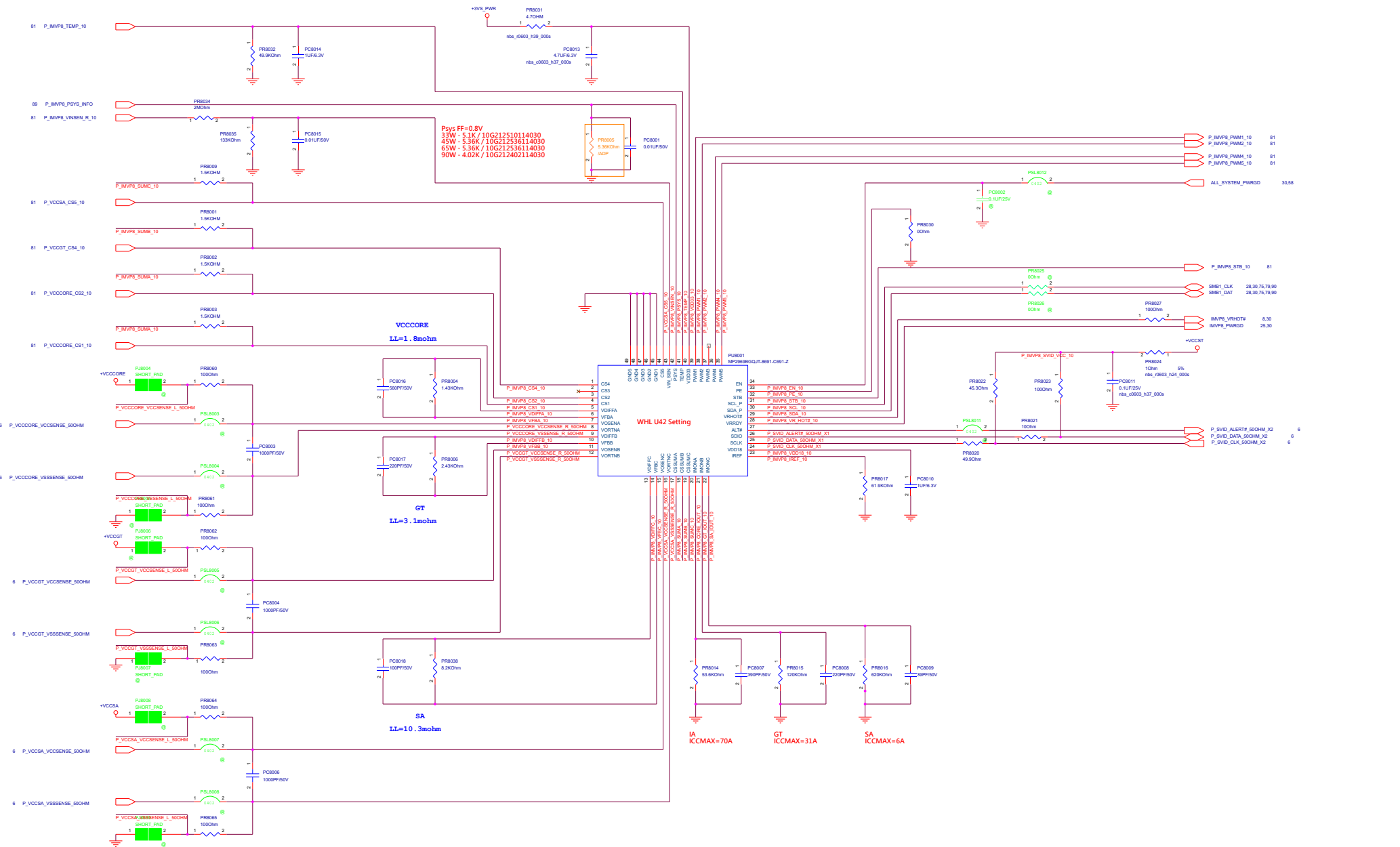


Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
R7905	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
R7906	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

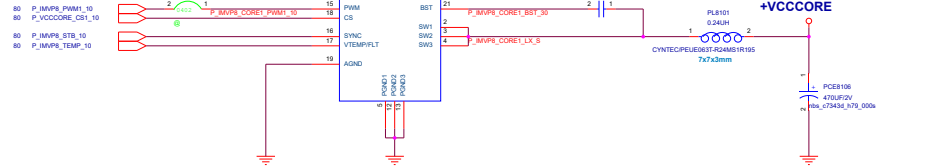
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WHL IMVP8 (1) Power [For CPU]

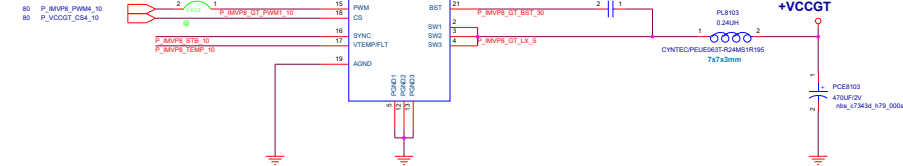


WHL IMP8 (2) Power [For CPU]

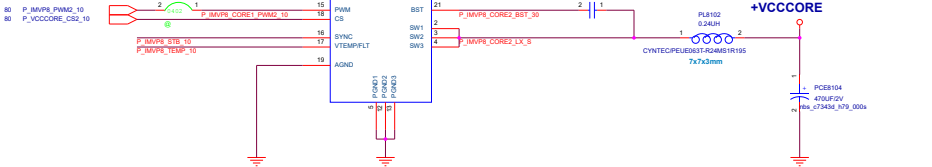
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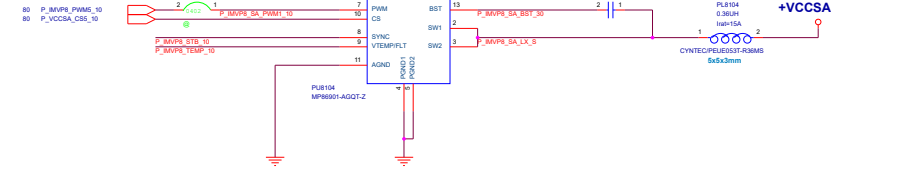
PWM與CS隔20mil



PWM與CS隔20mil

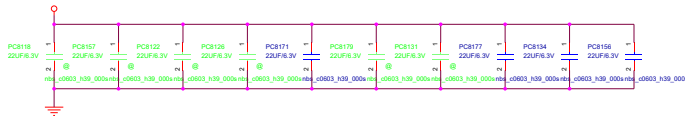


PWM與CS隔20mil



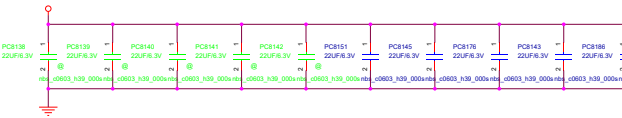
+VCCORE

10PCS / 10PCS



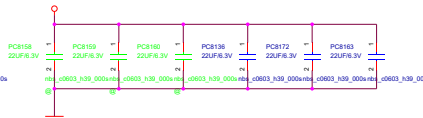
+VCCGT

10PCS / 5PCS

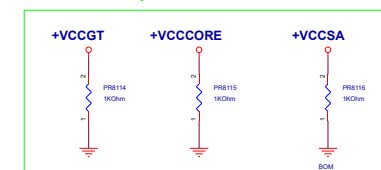



+VCCSA

6PCS / 3PCS

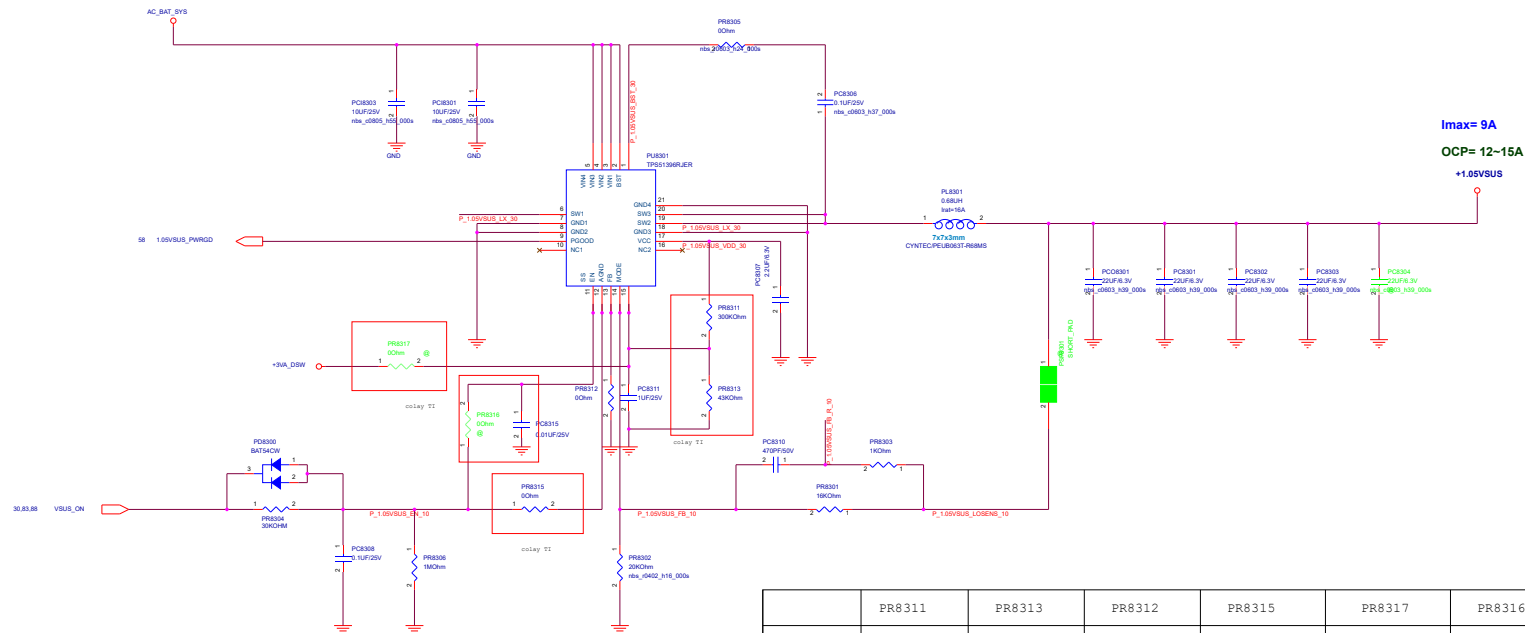


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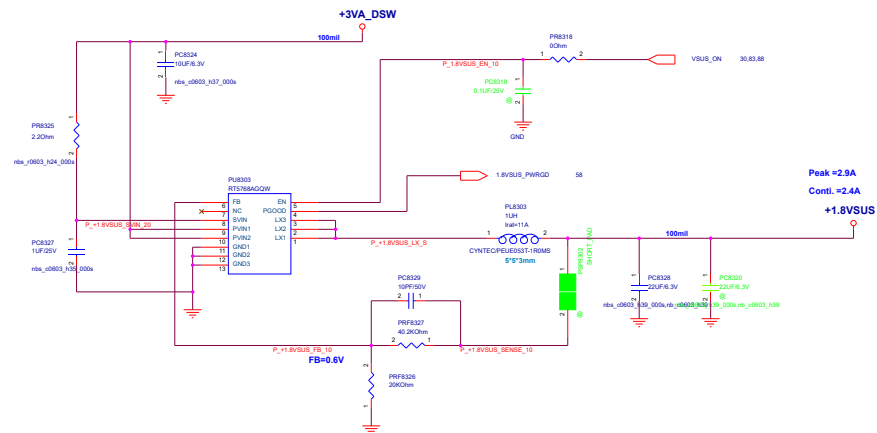


		Project Name		Rev
		UX334F		R2.0
Title : PW_				
Size	Dept.:		Engineer:	
A	NB Power team		SS	
Date: Wednesday, April 10, 2019			Sheet	82 of 102

+1.05VSUS [For PCH]




+1.8VSUS [For PCH]




©Core Design

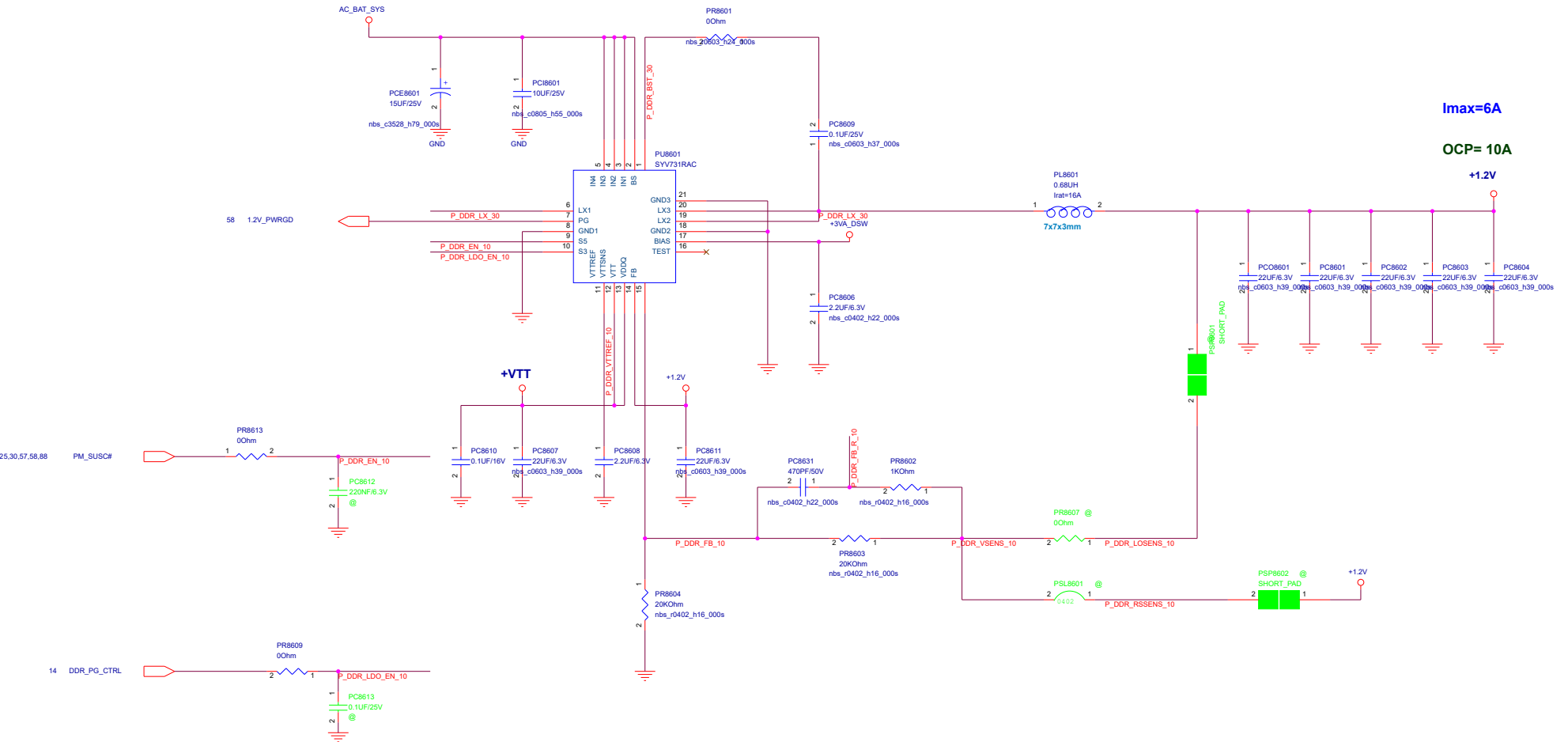
<Variant Name>

		Project Name		Rev
		UX334F		R2.0
Title : PW_				
Size	Dept.:		Engineer:	
A3	ASUS		SS	
Date: Wednesday, April 10, 2019			Sheet	84 of 102

<Variant Name>

		Project Name		Rev
		UX334F		R2.0
Title : PW_				
Size	Dept.:		Engineer:	
A3	ASUS		SS	
Date: Wednesday, April 10, 2019			Sheet	85 of 102

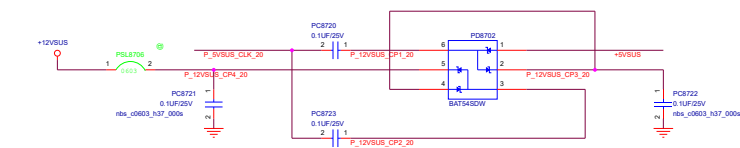
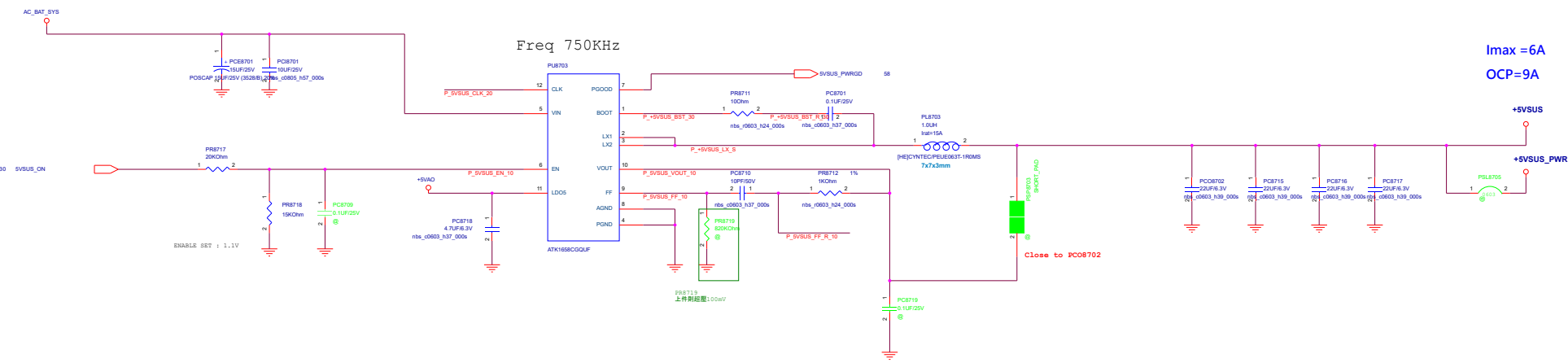
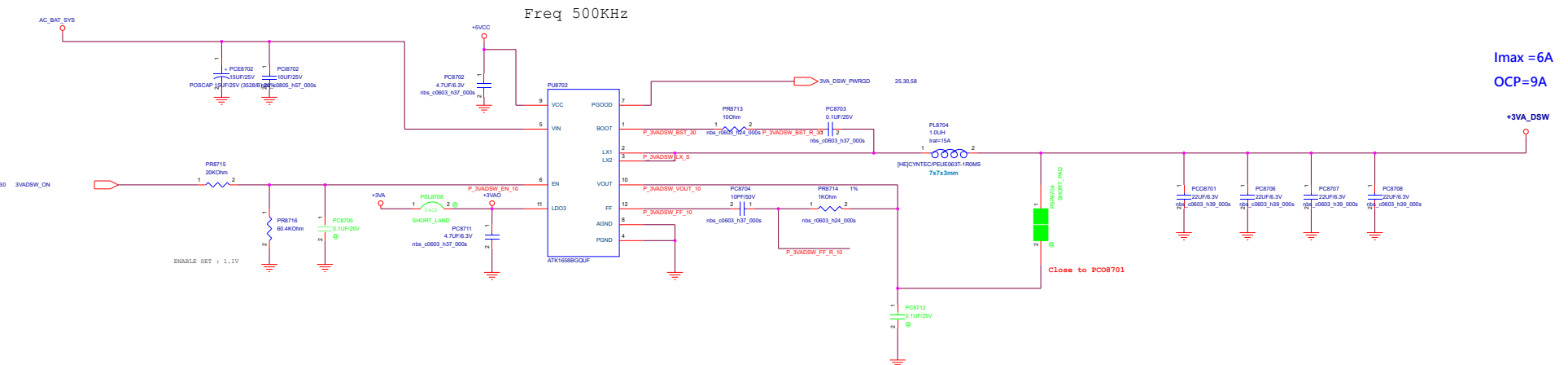
+1.2V / +VTT[For Memory]

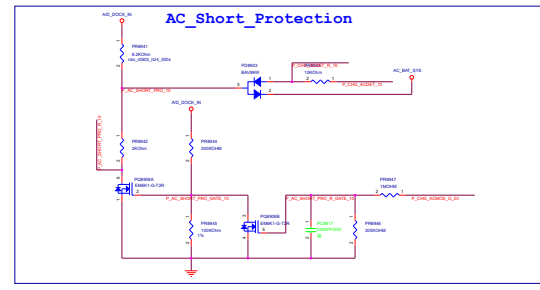
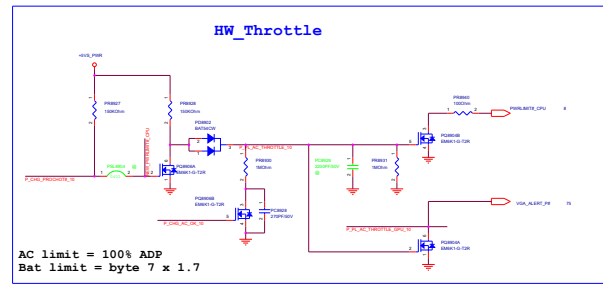
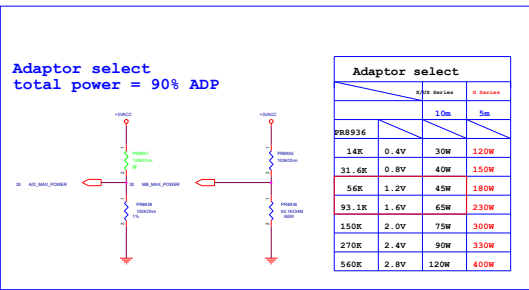
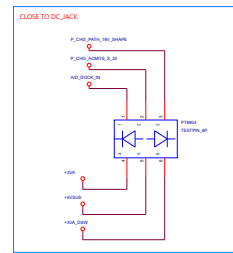
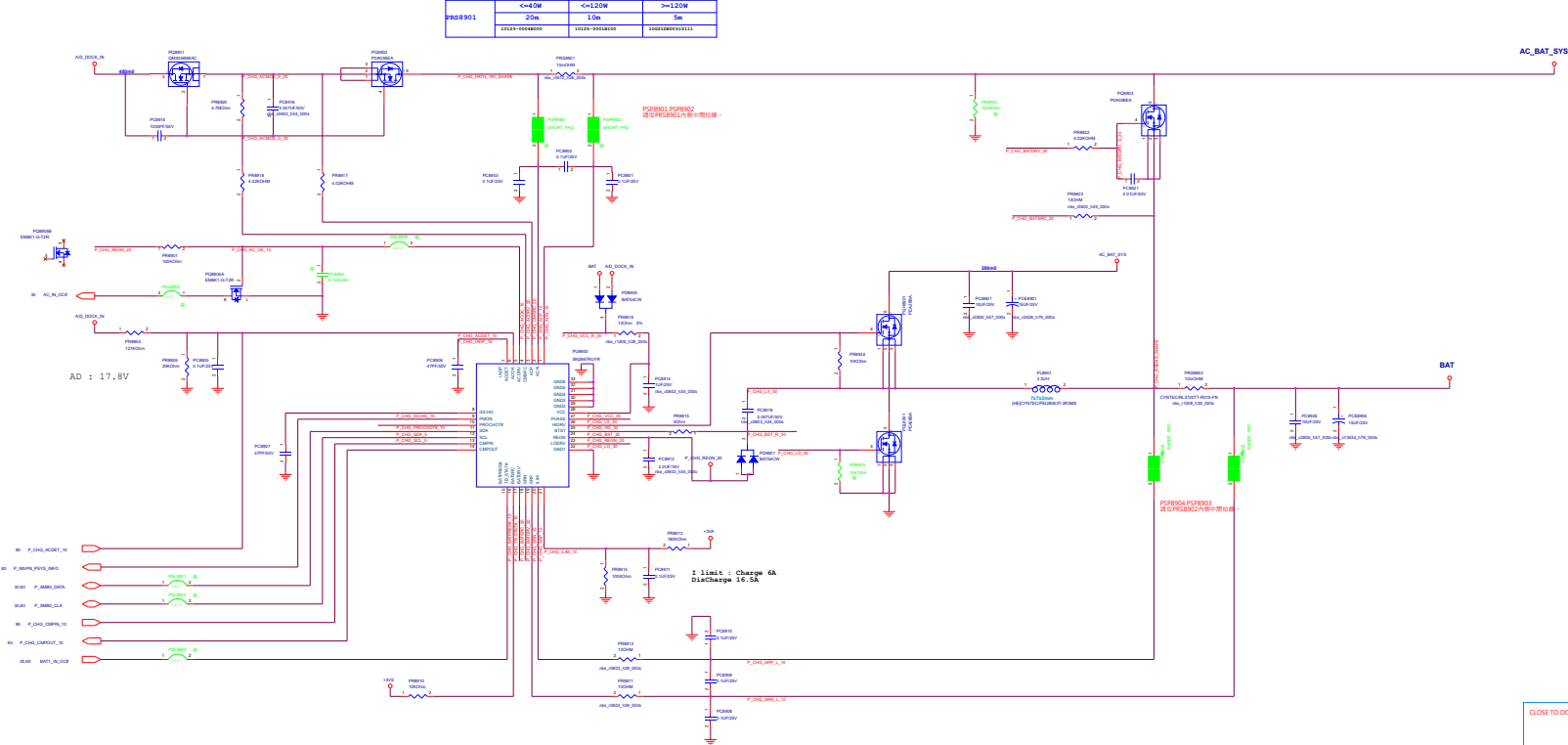


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		Project Name	UX334FN	Rev	R1.0
Title : PW_+1.2V/+VTT					
Size	A3	Dept.:	ASUS	Engineer:	Jerry Lai
Date:	Wednesday, April 10, 2019	Sheet	86	of	103

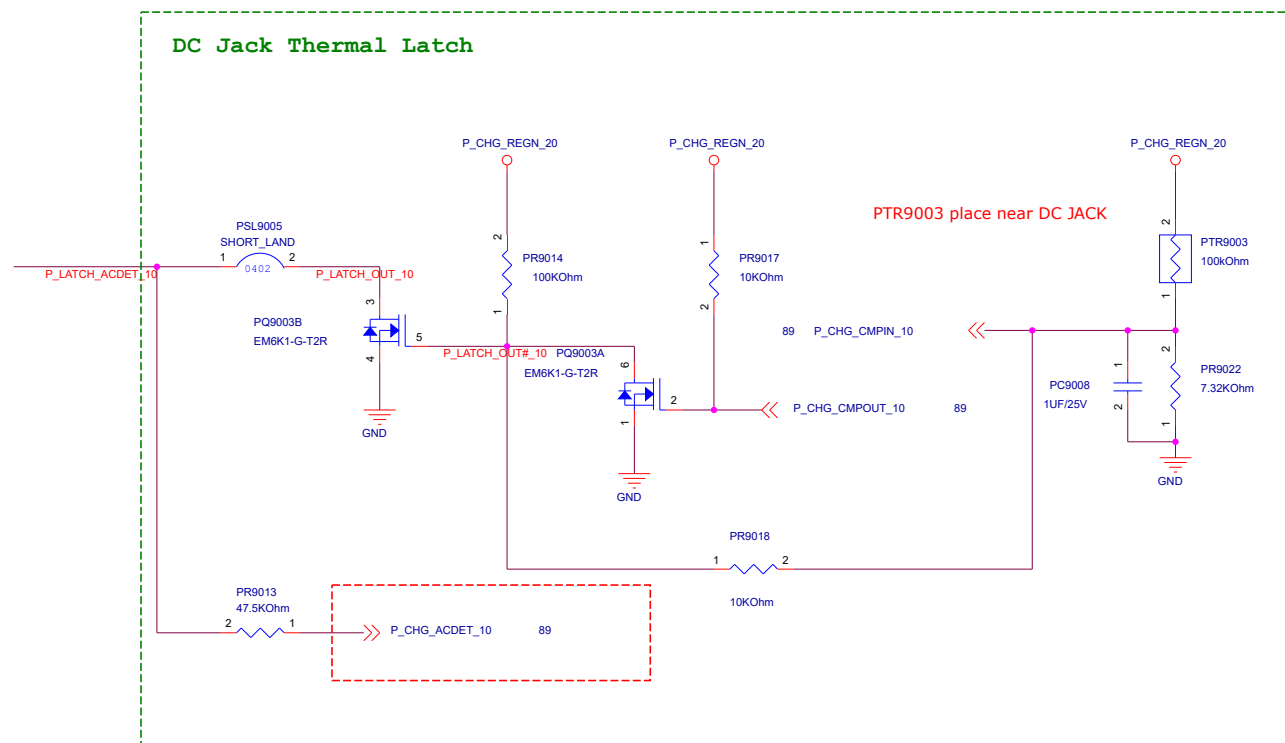
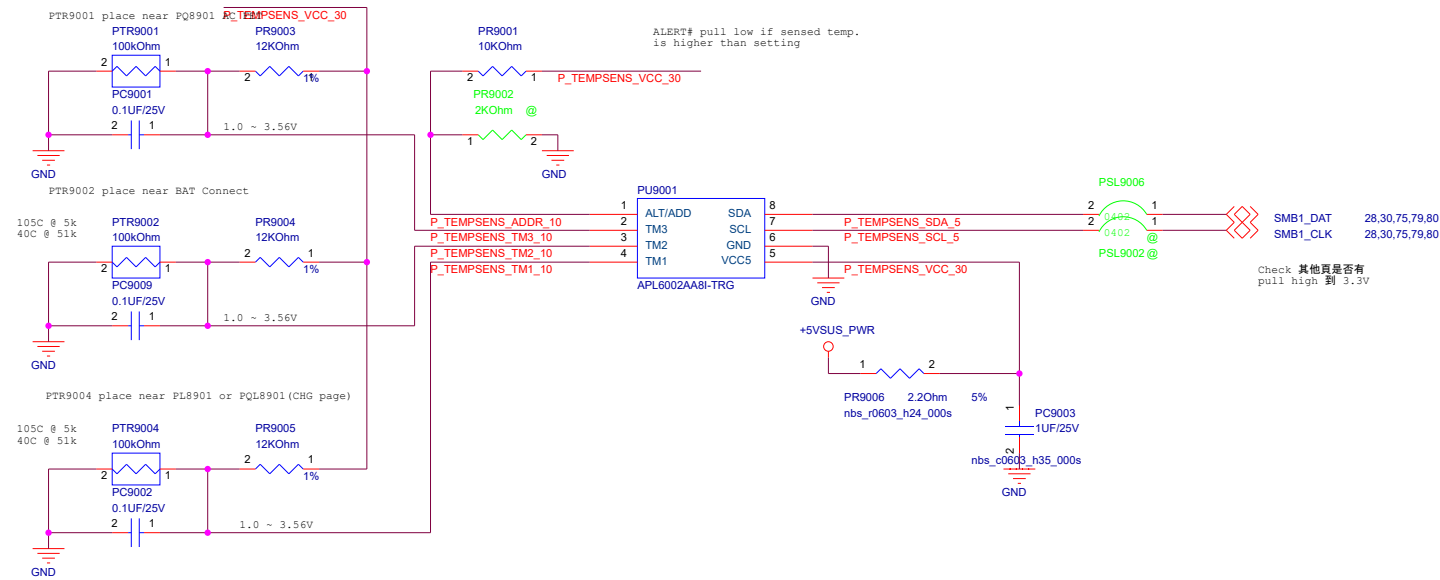
+3VA_DSW / +5VSUS [System Power]



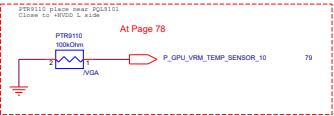


Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Address	0x00 0x01 0x02	0x03 0x04 0x05	0x06
R/W	W W W	R R R	R
Function	Temp. alert threshold setting	Sensed temp. data	bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert



+NVVDD [For DGPU]



79

Fsw	RT8820A
495K Hz	PR9115 309KOhm
350K Hz	PR9115 620KOhm

close to GPU

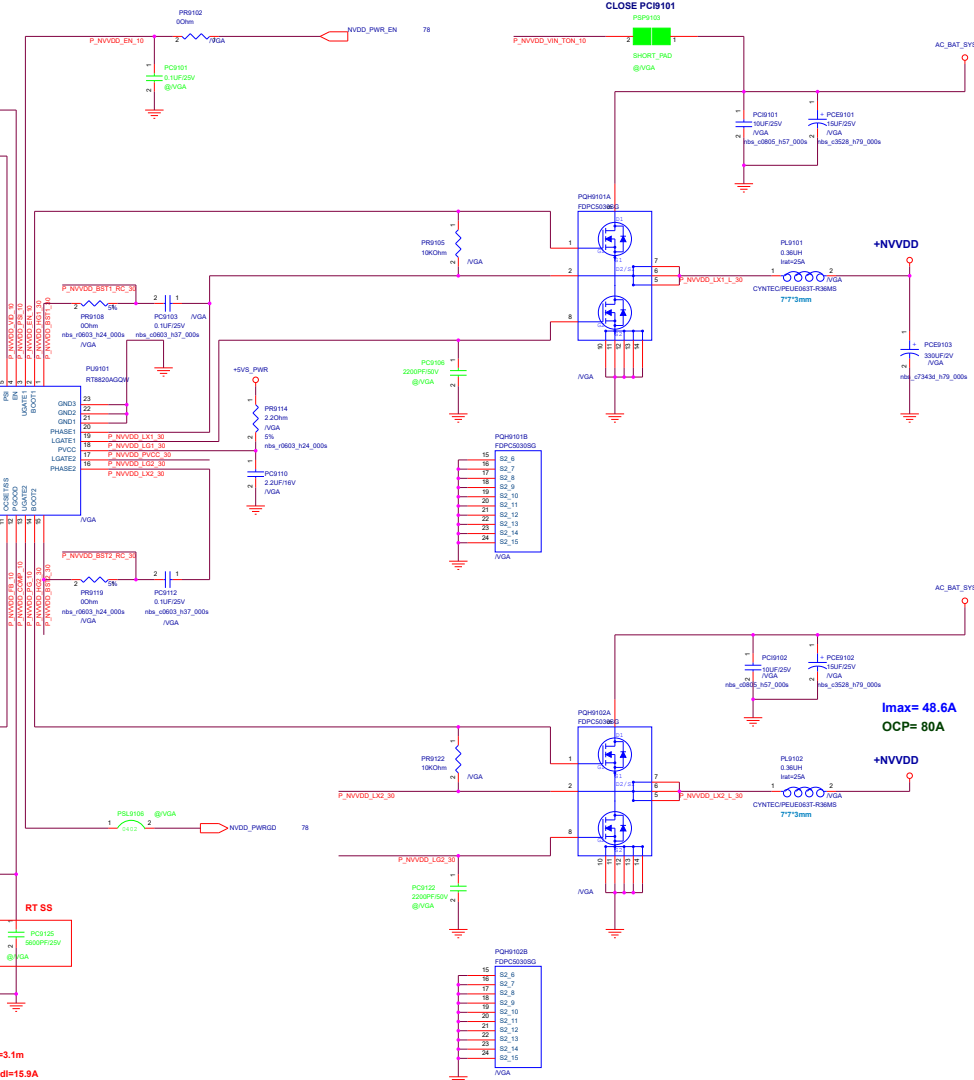
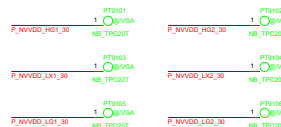
PSP9101 & +NVVDD CLOSE PCE9102

算式為Per Phase
 $ROC = \text{valley} \cdot R_{ds} \cdot I^2 / 10uA$
 RT OCL=80A


OCF=100A	RT8820A
QK3056*2	PR9128 1.78KOhm
AC06*2	PR9128 1.78KOhm

QM3056*2 Ron=6.22mΩ
 L=0.22u ; f=250KHz ; di=15.9A
 L=0.36u ; f=250KHz ; di=8.6A

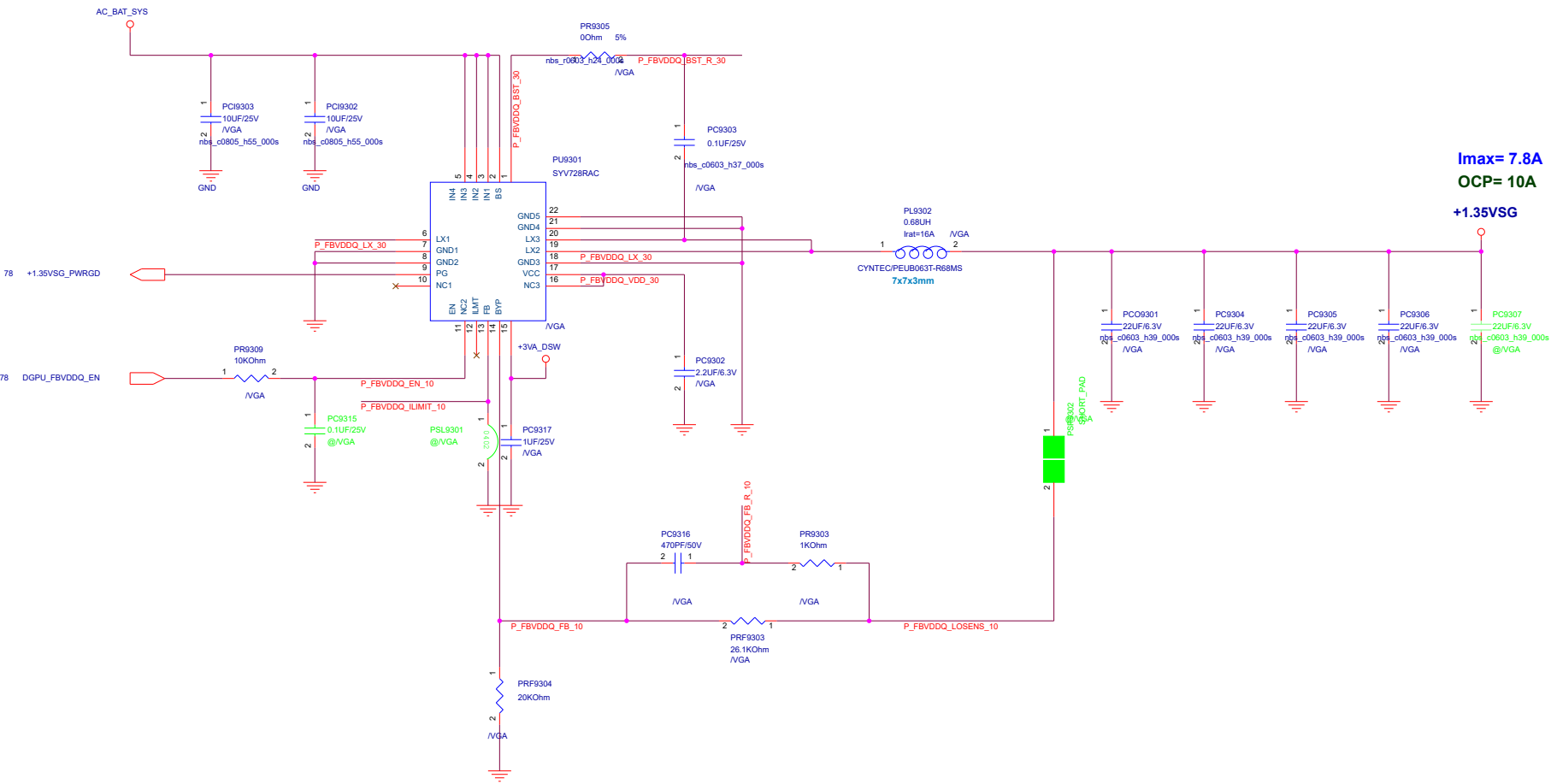
PT910* 請放置 PU9101旁;並請放置Trace 上!



<Variant Name>

		Project Name		Rev
		UX334F		R2.0
Title : POWER				
Size Custom	Dept.: ASUS		Engineer:	SS
Date: Wednesday, April 10, 2019			Sheet 92	of 102

+FBVDDQ [For VRAM]



<Core Design>

		Project Name	Rev
Title : PW_+FBVDDQ		UX334FN	R1.0
Size	Dept.:	Engineer:	
A3	NB Power team	Jerry Lai	
Date:	Wednesday, April 10, 2019	Sheet	93 of 102

<Variant Name>

	Project Name UX334F	Rev R2.0
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Title : POWER

Size Custom	Dept.: ASUS	Engineer: SS
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Date: Wednesday, April 10, 2019	Sheet 94 of 102
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	Project Name UX334F	Rev R2.0
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Title : POWER


Size Custom	Dept.: ASUS	Engineer: SS
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Date: Wednesday, April 10, 2019	Sheet 95 of 102
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<Variant Name>

		Project Name		Rev	
		UX334F		R2.0	
Title : POWER					
Size Custom	Dept.: ASUS		Engineer:		SS
Date: Wednesday, April 10, 2019			Sheet	96	of 102

<Variant Name>

		Project Name		Rev	
		UX334F		R2.0	
Title : POWER					
Size Custom	Dept.:	ASUS	Engineer:	SS	
Date: Wednesday, April 10, 2019			Sheet	97	of 102

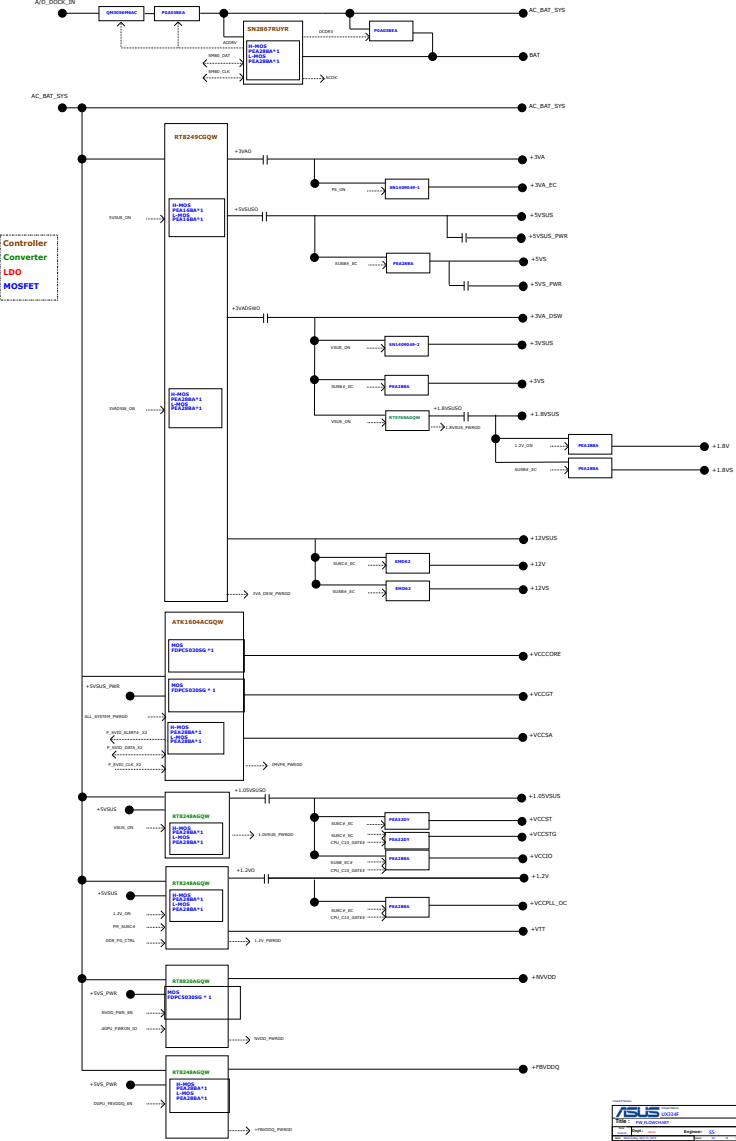
<Variant Name>

	Project Name UX334F	Rev R2.0
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Title : POWER

Size A3	Dept.: ASUS	Engineer: SS
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Date: Wednesday, April 10, 2019	Sheet 98 of 102
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Power-On Sequence Timing Diagram Rev.0.1

For Detail power sequence timing spec,
please refer to #543016 chapter 43

